# DPR-120 DP Reference Sink with Debug and Test Controller GUI



# **USER MANUAL**

# /// UNIGRAF

DPR-120 User Manual

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DPR-120 User Manual

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DPR-120 meets the essential health and safety requirements, is in conformity with and the CE marking has been applied according to the relevant EU Directives using the relevant section of the corresponding standards and other normative documents.

UNIGRAF DPR-120 User Manual

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# 1. ABOUT THIS MANUAL

### Purpose

This guide is the User Manual of DPR-120 Reference Sink and DTC, Debug and Test Controller GUI for use in a PC with Windows® 8, Windows® 7 or Windows® XP operating system.

The purpose of this guide is to

- Give an overview of the product and its features.
- Give instruction for the user on how to install the software and the drivers.
- Introduce the HW features of the DPR-120 unit.
- Give instructions for the user how use the DTC GUI.

### **Product Version**

This manual explains features found in **Debug and Test Controller GUI, DPR-120 DTC version 1.11.** Please consult Unigraf for differences between versions.

Please consult the Release Notes document in the installation folder for details of the SW and FW versions and changes to previous releases.

### Notes

On certain sections of the manual, when important information or notification is given, text is formatted as follows. Please read these notes carefully.

Note

This text is an important note

# 2. INTRODUCTION

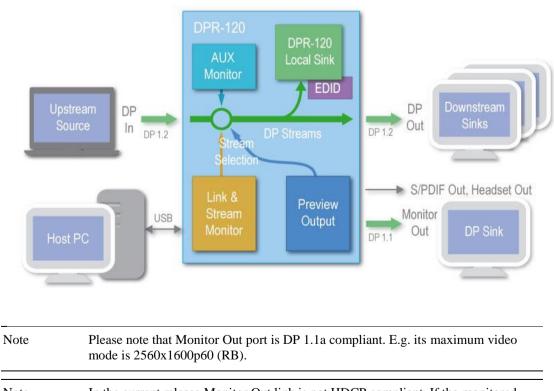
# **Product Description**

DPR-120 is a High Bit Rate 2 (HBR2) and Multi Streaming (MST) capable Reference Sink and branch device. Debug and Test Controller GUI (DTC) is a graphical user interface for DPR-120. Test Automation Shell and its API are an optional interface for automated testing.

- DP 1.2 compliant Reference Sink and Branch device
- Is able to recognize and monitor up to 4 DisplayPort Streams
- Local Sink functionality with DP 1.1 compliant monitor output
- Debug and Test Controller GUI with stream status monitoring and EDID and DPCD read write and edit functionalities.

# Functionality in a Nutshell

DPR-120 is a MST and HBR2 compatible DisplayPort Reference Sink and a configurable Display Port Sink and Branch Device. The GUI allows the user to configure the features of the Sink in order to test his Source or Sink DUT in different configuration scenarios.

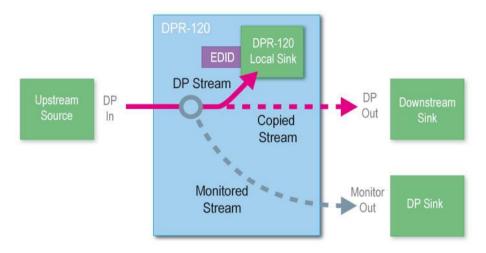


Note In the current release Monitor Out link is not HDCP compliant. If the monitored stream is HDCP encrypted, it will not be displayed on Monitor Out port.

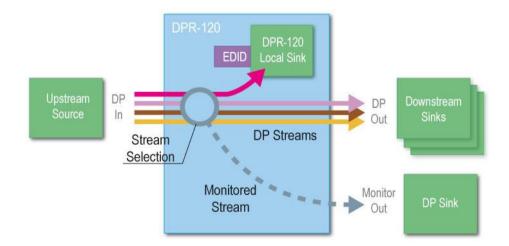
# SST and MST Modes

DPR-120 can operate either in Single stream (SST) mode or Multi stream (MST) mode. The selection is done with the **MST Capable** check box in *Main Link* tab in *DP Input* Group. Please find the description in Chapter 4 below.

In Single stream mode DPR-120 is seen as a single Local Sink. The local EDID and DPCD registers define its capabilities for the upstream source. The received stream for the Local sink is copied to **DP Out** port and also in the **Monitored Stream**.



In Multi stream mode, i.e. when **MST Capable** check box is selected in the GUI, DPR-120 is seen as a Multi-stream capable DP Sink. The received streams are forwarded according to the intent of the Upstream Source. In normal case one of the streams is for the *DPR-120 Local Sink* but this is not necessary the case. All four possible streams can be forwarded to downstream sinks as well.



Based on the **Stream Selection** on the *Main Link* tab in *DP Input* Group one of the input streams is selected for monitoring. The details of the stream is shown in the status fields of the Debug and Test Controller GUI and the stream is also forwarded to the *Monitor Out* port.

# Monitor Out Port

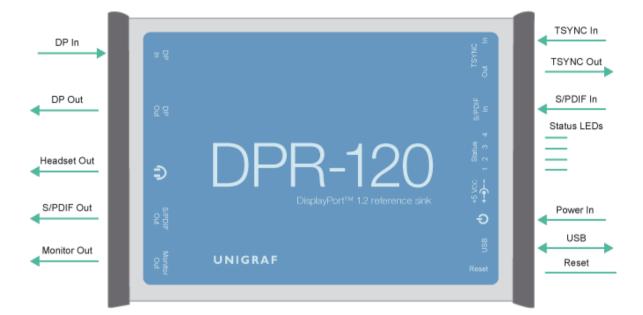
*Monitor Out* is a DP 1.1a compliant display output for monitoring the stream selected on the *Main Link* tab in *DP Input* Group. *Monitor Out* port does not support HDCP.

A copy of the monitored stream is fed to *Monitor Out* unscaled, as received. DPR-120 assumes that the monitor connected to the *Monitor Out* is able to support the stream.

Note:	Please note that <i>Monitor Out</i> port is limited to DP 1.1 capability (2560 x 1600 p60 (RB) resolution) only.
Note:	Please note that <i>Monitor Out</i> port is not detecting the display capabilities of the connected monitor. The stream selected on the <i>Main Link</i> tab in <i>DP Input</i> Group is output unchanged.
Note	Please note that <i>Monitor Out</i> does not support HDCP. An HDCP encrypted input video stream will not be output to this port.

# **DPR-120 Hardware Features**

The image below describes the connections and controls of DPR-120 and their description



Name	Description				
DP In	DisplayPort input from the upstream Source				
DP Out	DisplayPort output to the downstream Sink				
Monitor Out	Copy of the monitored DisplayPort stream.				
Headset Out Analog audio output. (Currently not in use)					
S/PDIF In	Optical audio input. (Currently not in use)				
S/PDIF Out	Optical audio output. Audio embedded in the monitored stream.				
Power In	+5 Vdc Power Supply Input				
USB	USB connection to the host PC				
Reset	Pushbutton to reset the unit				
Status LEDs	Status 1: HDCP Status Off = disabled				
	On = enabled				
	Status 2: Monitor Out				
	Status 3: DP Out				
	Status 4: DP In				
	<b>Off</b> = Cable disconnected,				
	Blinking = Cable connected but no link,				
	On = Link training successful.				
TSYNC In	Synchronizing input. TBD				
TSYNC Out	Synchronizing output. TBD				

# 3. INSTALLATION

# Unpacking

The DPR-120 product shipment contains

- The DPR-120 unit
- AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +5 Vdc output)
- USB cable
- The Utilities CD containing the SW installer. An electronic copy of this User Manual is included.

# Contents of the Installation CD

The DPT-120 Installation CD contains DPR-120 Setup utility including the following items:

- Windows drivers (installed during set up)
- DPT-120 firmware matching the SW version included (embedded in the GUI application, automatically updated when GUI run)
- DPR-120 Debug and Test Controller software GUI (installed during set up)
- DPR-120 Test Automation Shell (optionally installed during set up)
- User Manuals including this document.

 Note:
 Please install the software before connecting the DPR-120 in your PC.

 Note:
 System administrator's privileges are required for performing the installation.

### Software Installation

Start the installation by running **DPR-120 Setup.exe** 

Once the installer has started a welcome page is displayed. The welcome page shows the software package release version.

- Click Next to continue. In the next dialogs you will able to define which software components are installed.
  - A fresh version of the DPR-120 DTC Application
  - Optionally the *Device Drivers*.

The next two dialogs will allow you to define the install folder in your PC and the Start Menu folder used.

- When you are ready with the selections, click **Install** to start the installation.
- Click **Finish** to exit installation.

# Firmware Update

The DPR-120 firmware matching with the DP DTC GUI SW is embedded in the GUI application code itself. When DP DTC application is launched the firmware version programmed in the hardware is automatically checked and updated if needed.

📀 Unigraf DP Debug and Test	Controller	
File Help		
	Writing Firmware: 1036304 Bytes to go	
	Cancel	
		h.

### License Keys

For some feature of the DPR-120 you will need a hardware specific license key. Each license is valid for one specific device only. By using the GUI you can read the *Seed Number* of your DPR-120 unit. For a given Seed Number, Unigraf will provide you a *License Key* that will enable you to use the GUI from any PC to control your DPR-120.

You can usually find your License Key printed in a sticker that can be: glued on the unit's enclosure, included in the delivery package or among its related documents. If you cannot locate the License Key, please contact Unigraf and provide the Seed Number shown on the dialog in order to receive your License Key.

The Basic Debugging features of the DPR-120 do not require a license keys. When purchasing additional features like Compliance Test Tools and Test Automation Shell, you will be provided the license key matching the new features. The key will enable the corresponding features in the DP DTC GUI.

Insert each of the 32 character long License Keys in the field provided and click Add License. When you have inserted all licenses, click Proceed. The license keys are now saved in your PC and you can constantly use the device from this PC.

Jnigraf DP D Help	ebug and Test Controller				
					-
	Licenses installed for device DPR-120 [1:	350C369]			
	License	Кеу			
	<ul> <li>Φπ Generic Debug</li> <li>Φπ Test Automation Shell</li> </ul>	< Key Not Required > VNP9-4RAS-FUEV-MCCT-T4	LH-OF07-YH4R-FNOL		
	<ul> <li>ΦπLL CTS Extensions, Test set A+B+C</li> <li>ΦπMST Debug Extension</li> </ul>		PJ-72QT-NLXK-FQ5E		
	• πMST Debug Extension	E1K3-CKWQ-01KH-3D140-3	AKY-SERA-QRED-INQC		
	Remove selected		Device Seed number:	70777e70000000a9	
		<b>.</b>		Add License	
	www.unigraf.fi		Back	Proceed	

Note	Please note that each license is bound to one specific DPR-120 unit. The same license can be used with any number of PCs.
Note	The License Key never includes characters I, G, B, O because of their similarity with the corresponding numbers. If in doubt, please use numbers. You can use copy and paste to insert the License Key.
Note	The DPR-120 unit must be connected to your PC for entering the License Key.

# 4. DEBUG AND TEST CONTROLLER GUI

Debug and Test Controller GUI (DTC) is the user interface for DPR-120. The various functionalities are divided into groups and tabs providing the user in each tab functions related a certain task or operation. Some of the functions need a license and the related groups are visible in the GUI only when a valid license key has been entered.

The following chapters describe the contents of the DTC and the related functions.

**DP Input** monitors the status and the functions related to the *DP Input* interface from the upstream Source Device. The user can monitor the streams received by DPR-120. This group is always visible and is not enabled by a license.

**Terminal** is a tool for running embedded DPR-120 commands.

Source DUT Testing is the group for running CTS Tests

### **DP Input Group**

This tab has six tabs, each dedicated to a certain function.

### Main Link Tab

Main Link tab contains four panels: *Link Status, Link Configuration, Stream Status and optionally Streams / Timeslot allocation* (enabled with a license).

P Input Terminal Source D	UT Testing		
ain Link E-EDID MSA Log CR	C Log DPCD AUX		
Link Status		Link Configuration	
Lane 0 Lane 1 Lane 2	Lane 3	Max. Lane count	
	Clock Recovery	1 Lane	anes 💿 4 Lanes
	Symbol lock Channel equalization	Max. Link rate	
400 400 400	400 Voltage swing (mVpp)	1.62 Gbps	0 Gbps
3.5 3.5 3.5	3.5 Pre-emphasis (dB)		
0x0000 0x0000 0x0000	0x0000 Error Count (Click to dea	r) MST Capable	
Lane count: 4	Bit rate (Gbps): 5.4 (	HBR2) Generate HPD pulse on Apply	Apply Changes
Framing mode: Enhanced	Scrambling: Enab	led	
MST mode: Enabled			Update Link Status
14CD TD 001	NOD ID 002		
VCP ID 0x01 1 Port ID 0x08 PBN = 0x04b1	31 VCP ID 0x02 32 Port ID 0x00 PBN = 0x04b1	62 63 Not 64	
1 Port ID 0x08     PBN = 0x04b1     Stream Status     Monitored stream: VCP II     Horizontal	31 32 Port ID 0x00 PBN = 0x0401 0 0x01 •	Video Signal Status	CRC
Port ID 0x08     PBN = 0x04b1     Stream Status     Monitored stream: VCP II     Horizontal     Total: 2720	31 32 Port ID 0x00 PBN = 0x04b1 0 0x01 • Vertical Total: 1646	Video Signal Status	Red CRC: 0xf7d3
Port ID 0x08     PBN = 0x04b1     Stream Status     Monitored stream: VCP II     Horizontal     Total: 2720	31 32 Port ID 0x00 PBN = 0x04b1 0 0x01 • Vertical Total: 1646	Video Signal Status Misc Color Encoding Format: RGB unsp. (legacy RGB mode	Red CRC: 0x £7d3
1         Port ID 0x08           PBN = 0x04b1           Stream Status           Monitored stream:         VCP II           Horizontal         Total:         2720           Start:         112	31 32 Port ID 0x00 PBN = 0x0401 0 0x01 • Vertical Total: 1646 Start: 43	Video Signal Status Misc Color Encoding Format: RGB unsp. (legacy RGB mode Color Depth per Channel:	Red CRC: 0xf7d3 ) Green CRC: 0xcd5b

#### Link Status

Link Status displays the status of the link training and the link parameters negotiated between the DPR-120 Sink and the Upstream Source. The data is retrieved from the DPCD registers of the DPR-120 Sink. The status is updated automatically.

#### Link Configuration

Link Configuration allows the user to change the way the Sink capabilities are announced in the DPCD registers of the DPR-120 Sink. *Maximum Lane Count* and the *Maximum Link Rate* are set with their appropriate radio buttons. For enabling the *Multi Streaming* (MST) support select the **MST Capable** check-box.

To update the new status to the DPCD registers click Apply Changes.

To apply a *Hot Plug Detect* pulse automatically after updating the status, select **Generate HPD pulse on Apply**. HPD pulse duration will be defined in the *Bottom Panel*.

#### Stream / Timeslot Allocation

Streams / Timeslot Allocation panel is enabled with *MST Debug Extension* license key. The panel shows the time slot allocation for the various MST stream payloads in the received upstream link. In case of SST operation, the panel is empty.

Streams / Timeslot allocation

VCP ID 0x01 VCP ID 0x02 1 Port ID 0x08 31 32 Port ID 0x00 62 PBN = 0x04b1 64 Used 64
PBN = 0X04D1 PBN = 0X04D1

In the example case above, time slots 1 to 31 have been allocated to VC Payload (VCP, Virtual Channel Payload) 1 and time slots 32 to VC Payload 2. Time slots 63 and 64 are unallocated.

Port number for VC Payload 1 is 0x08 and for VC 2 0x00. The Payload Bandwith Number for both payloads is 0x04b1.

#### Stream Status

<u>Video Signal Status</u> information is retrieved from the DPR-120 Local Sink input measurement block. It indicates if valid video is received in the stream.

Note:	DPR-120 video signal status is based on the capabilities of the used STDP9320 chip. The chip can only process timings up to 4K30Hz. This LED will not provide any meaningful information for pixel clock timings exceeding 4K30Hz.
	<u>Video Timing Details</u> are retrieved from the Main Stream Attributes (MSA) of the monitored stream.
Note:	Please note that the MSA information used for <i>Video Timing Details</i> is provided by the Upstream Source, it is not measured by the DPR-120 Local Sink.
	The 16-bit CRC values of the three color components calculated by the Sink hardware 1

The 16-bit <u>CRC</u> values of the three color components calculated by the Sink hardware. To re-read, click **Update**.

### **Bottom Panel**

The bottom panel of the dialog is shown in all tabs of the *DP Input* group. It includes the controls for the Hot Plug Detect (HPD) signal.

To apply a HPD Pulse with programmable duration click **Pulse HPD**. The duration will be defined in the provided field.

For applying a short pulse click **Short Pulse HPD**. Pulse duration is 1 ms.

Clicking the **De-assert HPD** button will cause HPD line be set to low (de-asserted) and hence no HPD pulse can be generated while HPD line set to low. Click the **Assert HPD** to re-activate (assert) the HPD line.

Total: Start: Active: Sync Width:	2720 112 2560 (+) 32	Total: Start: Active: Sync Width:	1646 43 1600 (+)6	Color Encoding Format: RGB unsp. (legacy RGB mode) Color Depth per Channel: 10	Red CRC: Green CRC: Blue CRC:	0x6be8 0xc0fa 0xe1c7
Assert HPD	"Lr Pul	se HPD Pulse Du	ation: 1000	Short Pulse HPD		

### E-EDID Tab

This tab provides tools for accessing the EDID of the DPR-120 Local Sink presented to the Upstream Source Device. There are three basic functions:

- Load and save EDID data files in the host PC
- Edit the EDID contents
- Program and read the contents of the hardware EDID memory

le Help																	
PInput	Termina	S	ource D	UT Test	ling												
lain Link	E-EDID	MSA L	og CR	C Log	DPCD	AU	Х										
ID Data:																	
00000	00 ff	ff ff	ff f		0 54	c7 3	6 40	4c 3	34 3	2 30	~	٦r	EDID Files				
000010	14 16	01 04	b5 4	1 2 9 7	78 22	8f 9	5 ad	4f 3	32 b	2 2 5	Π		Load		Save as	Defe	It EDID
000020											ш	Ц	Load		Save as	Derau	IT EDID
000030											ш	1	HEX Editor				
000040												L					
000050												L	Clear		Append file	EDID E	ditor
000070												Ľ					
080000												L					
000090	1f c0	00 00	00 0	0 00 0	00 00	00 0	0 00	00 0	0 0 0	0 00		L					
0000a0	00 00	00 00	00 0	0 00 0	00 00	00 0	0 00	00 0	0 0 0	0 00		L					
0000b0	00 00	00 00	00 0	0 00 0	00 00	00 0	0 00	00 0	0 0 0	0 00		L					
0000c0												L					
0000d0												L					
0000e0											=	L					
0000£0	00 00	00 00	00 0	0 00 0	00 00	00 0	0 00	00 0	000	0 80		L					
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												L					
													Device EDID				
												I	Device CDID				
													Read		Write		
											Ŧ						
		_				_					-	-		_			
De-as	sert HPD		U	Pulse i	HPD	Pu	lse Du	ation	: 10	00	*	ms	T Short Pulse HPD				

#### **EDID** Files

With **Load...** and **Save as...** you can read and write a hex EDID file from your PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

Note Currently the EDID Editor does not support Display ID. You can however modify hex EDID files with the HEX Editor or load and program externally generated hex EDID files that have Display ID content.

#### **HEX Editor**

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. You can edit the EDID contents by typing over the existing values. The altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

Once you are done with editing the data, you can either save it to an \*.ecd file in your PC with **Save as...** or program it to the hardware EDID memory with **Write**.



#### **EDID Editor**

You can edit the EDID structures of the data in the *HEX Editor* by clicking **EDID Editor**. EDID Editor is launched in a separate pop-up window.

O EDID_Editor				
E-EDID Encoder / Decoder				
Collection 1     Blocks in collection		Details of ":/0/Version/Vendor _Product ID"		
Blocks in collection     A · Block 0 [VESA EDID]		Кеу	Value	
Checksum		ID Manufacturer Name	UFG	
▲ · Version		ID Product Code	0x4036	
Extension flag		ID Serial Number	0x3032344c	
Vendor & Product ID				
Basic Display Parameters and Feature		Manufacture or Model year	Manufacture Year and Week	
Display x, y Chromacity coordinates		Handractare of Hodel year	Manafactare rear and week	
▷ · Established timings I and II ▷ · Manufacturer's Timings		Week of manufacture	Week 20	
> Standard Timings		Year of manufacture	Year 2012	
▲ 18-Byte data blocks		Year of manufacture	Year 2012	
▷ Descriptor 1				
Descriptor 2				
▷ · Descriptor 3				
▷ · Descriptor 4				
Block 1 [CEA 861]				
Checksum	4			
<ul> <li>CEA Extensions Version</li> <li>Sink Underscaps IT video</li> </ul>	L			
Basic audio	L			
	L			
	L			
	1			
Coad Save Show Hex		Show Log		

#### The Main Window

The *EDID Editor* main window is divided into three logical areas. The bottom part of the window contains the command buttons, and the log view. The top-left portion shows the currently edited E-EDID blocks in a tree-form, and the top-right portion shows an edit control for the currently selected item, possibly a list of sub-keys and their names (The list is not shown for all values) and the HEX-view of the block collection.

#### Command Buttons

**Load:** Load an EDID block collection file from disk. **Save:** Save the current block collection to a disk file. **Show Hex:** Show or Hide the HEX view. **Show Log:** Show or Hide the Log view.

#### **EDID Editor Features**

The EDID Editor currently supports VESA E-EDID block versions 1.3 and 1.4. As the standard defines, the versions 1.0, 1.1 and 1.2 are supposed to be backward compatible, and therefore the VESA E-EDID decoder will also show their contents. However, in these cases it should be noted that the error checking is not compliant with restrictions given in these older versions of the standard. In addition to VESA E-EDID block, the CEA-861 versions 1, 2 and 3 EDID blocks are also fully supported as well as the VESA Block Map Extension blocks.

Practically unlimited number of extension blocks may exist in a single collection. The number of blocks is limited by VESA Specifications and possibly by available system resources. Most EDID blocks contain a structure that is very similar to a tree-structure. The EDID Editor decodes each block into a tree-view of the block. The tree-view then contains all values contained within the EDID block. The contents can then be easily browsed, using only a few mouse clicks. The EDID Editor has a support for automatic variables, such as the block checksum. When the user changes a value in an EDID block, the tool will update the checksum accordingly. The automatic variables appear as read only values for the user. A log print will be made when an automatic variable is updated by the editor.

**HEX View**: An optional HEX data display of all blocks in the collection. The view also shows the latest changes highlighted.

**LOG View**: An optional LOG view, which will contain log prints generated by the editor. Mostly it will list values that have been automatically updated due to edits.

#### Editing tips

Editing an EDID block is very straightforward, but there are some special cases where the user must know how to accomplish certain types of tasks.

- Enter key will apply text-edit values and combo-box selection.
- To apply new setting to *binary* values (ones that show a check-box), please click the **Set** button.
- When you see a **Quick Config** button appear below an editor, you can access a configuration menu that allows you to quickly select one of multiple pre-defined setup options.
- In CEA-861 blocks, you can add and remove 18-byte descriptors and CEA data blocks by setting the values "18-byte Descriptors in this block" and "CEA Data block count". Unfortunately re-arranging the descriptors and CEA data blocks is not supported yet, so you need to be careful when editing these.
- Enter hex values with prefix "0x" or "\$", no prefix means a decimal value.
- You can always enter HEX or DEC, even if the value is presented as HEX, and/or value range is given in HEX.
- Floating point values must be given with period "." as decimal separator, even if your localization setting defines decimal separator as comma (or other).
- Remember to click **Set** after changing a bit-value presented as a single check-box if you want the new value applied.

Note It is recommended that you back up the un-edited EDID contents to a file before editing and writing it to the card.

#### Saving EDID Data

When you are done with editing you can either save the EDID contents to a file in the PC or bring it in the *HEX Editor*.

For saving the data to a file in your PC click Save.

For bringing the data to the HEX Editor close the EDID Editor window by clicking the **Window Close** button in the top right hand corner of the window. You will be asked if you would like to copy and replace the EDID data in the HEX Editor. Click **Yes** to replace the data, click **No** to discard the modifications.

When you are back in the *HEX Editor*, the bytes that the *EDID Editor* changed are highlighted with **BLUE BACKGROUND**.

### MSA Log Tab

MSA Log collects video status information from the stream selected In the *Main Stream* tab. The data will be stored since the DTC GUI was launched or **Clear** was clicked.

Click **Columns...** to select which data fields are shown. Please find a list of available fields and their column labels below:

ile Help	1											
P Input	Terminal	Source	e DUT Test	ing								
lain Link	E-EDID	MSA Log	CRC Log	DPCD	AUX							
Co	lumns	1							1	Save	Clear	
Daut Marchan		9										7
Timestam	p VC	PID	VSTAT		HACT	VACT	CEF		BPC			ł
7869130	MST	1: 1	Off		2560	1600	RGB unsp.	(legacy RG8 mode)	10			
7870601	n/a		On		2560	1600	RGB unsp.	(legacy RGB mode)	10			
7873774	n/a		Off		2560	1600		(legacy RGB mode)	10			
7875224			On		2560	1600	RGB unsp.	(legacy RGB mode)	10			
7924307			Off		2560	1600		(legacy RGB mode)	10			
7924310			On		2560	1600		(legacy RGB mode)	10			
7932442			Off		2560	1600	RGB unsp.	(legacy RGB mode)	10			
7932448	MST	: 2	On		1920	1200	RGB unsp.	(legacy RGB mode)	10			
De-as	sert HPD		T Pulse I	HPD	Pulse Dur	ation: 1000	ns T	* Short Pulse HPD				

Label	Description	Default
Timestamp	Timestamp in milliseconds from the re-start of the HW	✓
VCP IP	Virtual Channel Payload ID	✓
VSTAT	Video status (On / Off)	~
HPOL	Horizontal Sync polarity (+/-)	
НТОТ	Horizontal Total in pixels	
HS	Horizontal Start in pixels	
HACT	Horizontal Active in pixels	~
HSW	Horizontal Sync width in pixels	
VPOL	Vertical Sync polarity (+/-)	
VTOT	Vertical Total in lines	
VS	Vertical Start in lines	~
VACT	Vertical Active in lines	
VSW	Vertical Sync width in lines	
CEF	Color Encoding Format	✓
BPC	Color Depth per Channel	~

You can save the log in Comma Separated Values (\*.csv) format in your PC by clicking **Save**.

Note

When swapping between monitored streams, the first listing, indicating VSTAT=Off is caused by the monitoring circuitry. Please omit this listing.

### CRC Log Tab

CRC Log collects CRC values of the three color components of the received frames from the stream selected In the *Main Stream* tab. The logging is enabled by selecting the **Enable Logging** checkbox.

le Help							
P Input 1	erminal	Source D	UT Testing				
1ain Link E-	EDID M	SA Log CR	C Log DPCD A	UX			
Enable Log	ging					Save	Clear
Timestamp		VCP ID	Red CRC	Green CRC	Blue CRC		
7808813 7835125 7835588 7835588 7835934 7835934 7837950 7870750 7870750 7875224 787520 7911009 7911488 7911009 7911488 7911034 7911034 7922475 7922475 7922475		MST: 1 MST: 2 MST: 2 MST: 2 MST: 2	0xf7d3 0x0000 0x268d 0x05265 0xf7d3 0xf7d3 0xf7d3 0x6000 0x0000 0x0000 0x0000 0x0000 0x7d3 0x0000 0x076 0x2127 0xf7d3 0x6537 0xf7d3 0xf7d3 0xf7d3 0xf7d3 0xf7d3 0xf7d3	0xcd5b 0xf000 0x60a5 0x734e 0xcd5b 0xcd5b 0xcd5b 0x0000 0x719f 0x0000 0xcd5b 0x0000 0xcd5b 0x0000 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0xcd5b 0x	0x826f 0x0000 0xd15c 0x826f 0x7527 0x826f 0x0000 0x0000 0x0000 0x826f 0x0000 0x276 0x964f 0x826f 0x826f 0x826f 0x826f 0x826f 0x826f 0x826f		Ĩ
4							
•							
De-asser	t HPD	U U	Pulse HPD	Pulse Duration: 1000	ms Short Pulse HPC	D	

You can save the log in Comma Separated Values (\*.csv) format in your PC by clicking **Save**.



### DPCD Tab

DPCD tab is a tool for monitoring and editing the DPCD registers of the DPR-120 Sink.

The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

Ø Unigraf DP Debug and Test Controller	- • •
File Help	
DP Input Terminal Source DUT Testing	
Main Link E-EDID MSA Log CRC Log DPCD AUX	
DPCD Decoder 1.2 + DETAILED_CAP_INFO_AVAIL = 1	Clear
DPCD Address range: 0x 00 Number of bytes to read: 0x 100	
000000 12 14 c4 01 01 00 01 80 00 00 00 00 00 00 00 00 00 00 00 00	A
000010 00 00 00 00 00 00 00 00 00 00 00	
000020 00 01 00 00 00 00 00 00 00 00 00 00 00	
000030 a4 07 55 81 de 82 e5 11 b8 59 00 25 22 93 1a 45	
000040 00 00 00 00 00 00 00 00 00 00 00	
000050 00 00 00 00 00 00 00 00 00 00 00	
00 00 00 00 00 00 00 00 00 00 00 00 00	
00 00 00 00 00 00 00 00 00 00 00 00 00	
0000a0 00 00 00 00 00 00 00 00 00 00 00	
Set Reference 😰 Refresh 🗳 Write Changes	
DPCD Address range: 0x 200 Number of bytes to read: 0x 80	
000200 02 00 77 77 81 00 44 44 00 00 00 00 00 00 00 00 00	
000210 00 80 00 80 00 80 00 80 00 00 00 00 00	
000220 00 00 00 00 00 00 00 00 00 00 00	
000230 00 00 00 00 00 00 00 00 00 00 00 00 0	
000240 cf 11 9b 9c 21 40 20 00 00 00 00 00 00 00 00 00	
000250 00 00 00 00 00 00 00 00 00 00 00 00 0	
Set Reference 😨 Refresh	-
De-assert HPD Pulse HPD Pulse Duration: 1000 🖕 ms	

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

Main Link E-EDID MSA Log CR	C Log DPCD	
DPCD Decoder 1.2 + DETAILED_C	AP_INFO_AVAIL = 1	Load Save 🗍 Clear
DPCD Address range: 0x 0	Number of bytes to read: 0x 100	
000010 00 00 00 00 00 00	1 01 81 00 00 00 00 00 00 00 00 00 0 00 00 00 0	·
000040 00 00 00 00 00 00	0 00 00 20 c7 19 95 00 00 00 03 0 00 00 00 00 00 00 00 00 00 00 00 00 0 00 0	
Set Reference	Refresh 🛛 😽 Write Changes	

In the combo box above the DPCD Decoder window you can select how the DPCD data is interpreted, either as *DP 1.1 EDID*, or as *DP 1.2 EDID* with *Detailed Capability Info* selected or not (DETAILED\_CAP\_INFO\_AVAIL = 1/0).

- By clicking **Refresh** you can re-read the data from the DPCD registers to the window in question.
- By clicking Write Changes you can write the portion of data shown in the window in question to the DPCD registers.

• By clicking **Set Reference** you can store currently shown data as a reference for comparison.

When you refresh the data from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with red color.

Dunigraf DP Debug and Test Controller           File         Help           DP Input         Terminal         Source DUT Testing           Main Link         E-EDID         MSA Log         CRC Log         DPCD           DPCD Decoder         1.2 + DETAILED_CAP_INFO_AVAIL = 1 <ul> <li>Terminal</li> <li>Terminal</li> </ul>	🕞 💷 🕰
DPCD Address range: 0x 0         Number of bytes to read: 0x 100           000000         12 0a e4 01 01 01 01 81 00 00 00 00 00 00 00 00 00         00 00 00 00 00 00 00 00 00 00 00 00 00	LANED_1_STATUS [RO] (Lane0 and Lane1 Status) 0x00202 := 0x77 LANEO_CANNEL_EQ_DONE = 1 LANEO_STMPOL_LOCKED = 1 LANE1_CR_DONE = 1 LANE1_SYMBOL_LOCKED = 1 LANE1_SYMBOL_LOCKED = 1
Set Reference     Image: Refresh     Image: Write Changes       De-assert HPD     Image: Pulse HPD     Pulse Duration: 1000     Image: ms	Thort Pulse HPD

#### Saving and Loading DPCD Content

You can save the DPCD data in the address areas that you selected for the two windows as a file in your PC. You can save the content in three alternative formats:

- Binary *DPCD Fata File* format (\*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- Comma Separated Values (\*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (\*.HEX) in a human readable text format.
- By Clicking **Save** you will be able to select the location and the format of the file.
- ▶ By Clicking Load you can load DPCD data saved in *DPCD Data File* (\*.DPD) format to the editor.
- In order to program the data into the DPCD registers of DPR-120 Local Sink click Write Changes.

Note	- Writing DPCD data to the DPCD registers of the DPR-120 Local Sink will potentially affect the status and capabilities of DPR-120 as seen by the upstream
	source.
	- User control like Link Training or mode changes will modify the content of the DPCD registers
	- During a reboot of DPR-120 the DPCD registers will be returned to their default values.

### AUX Tab

AUX Tab is an AUX Channel Monitor for recording the AUX Channel traffic in the upstream link. The operation of this built-in AUX Monitor of DPR-120 is in many ways similar to Unigraf's *DPA-400 AUX Channel Monitor*. The advantage of the built-in function is that no extra connectors are used in the signal path that could potentially degrade the quality of the signal.

When acquisition is enabled, the AUX Channel Monitor collects all AUX Channel transaction between the upstream source and DPR-120. Each message is shown in the log dialog as time stamped raw data and also in its parsed form. In order to help the user compare the logged data to the specification, the parsed data is expressed with the same terminology used in VESA DisplayPort<sup>TM</sup> documentation.

Please refer to a full description of the AUX Channel Monitor features of in chapter <u>AUX</u> <u>Monitor</u> later in this document

The AUX Monitor function is enabled with MST Debug Extension license key.

Terminal	Source DUT To	esting				
E-EDID M	SA Log CRC Lo	g DPC	D AUX			
Chan a seculation						
Stop acquisite	on					
Timestamp	From	Type	Details	Data		Message details:
5710.02	DPR-120				*	Line #9 - 17263.01ms
17262.30						AUX_ACK - 14 bytes
17262.37	Sink				-	the state of the state
	Source					DPCD_REV [RO] (DPCD revision
17262.59	Sink			00 01		number)
17262.72	Source					0x00000 := 0x12
17262.78				00 07		DPCD V1.2
				90 00 00 0d		
						MAX_LINK_RATE [RO] (Maximum link
						rate of Main Link lanes)
						0x00001 := 0x14
						MAX_LINK_RATE = 5.4Gbps
						MAX_LANE_COUNT [RO] (Maximum
						number of lanes)
						0x00002 := 0xc4
						MAX_LANE_COUNT = 4
						ENHANCED_FRAME_CAP = 1
						TPS3_SUPPORTED = 1
						MAX_DOWNSPREAD [RO]
						0x00003 := 0x01
						MAX_DOWNSPREAD = 0.5%
						NO_AUX_HANDSHAKE_LINK_TRAINI
						NG = 0
17265.86	Source			80 10 00 04 10 02 cb 01 d5		NORP [RO] (Number of Receiver
17265.86	Source Trace	Side	DOWN_REQ - REQ: LINK_ADDR	10 02 cb 01 d5		DPCD Decoder mode:
17265.98	SINK	Native	AUX_ACK - U Dytes		٠	
concernation and the						1.2 + DETAILED_CAP_INFO_AVAIL = -
	Stop acquisitli Timestamp 7710.02 7262.30 7262.37 7262.37 7262.53 7262.53 7262.78 7263.26 7263.30 7263.30 7263.30 7263.31 7263.31 7263.32 7263.32 7263.32 7263.33 7263.43 7264.43 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.45 7264.36 7265.38 7265.36	Stop acquisition           Timestamp         From           7710.02         DPR-120           7262.33         Source           7262.34         Source           7262.35         Source           7262.37         Sink           7262.38         Source           7262.74         Source           7262.75         Source           7262.74         Source           7263.75         Source           7263.74         Source           7263.75         Source           7263.76         Source           7263.78         Sink           7263.79         Sink           7263.70         Sink           7263.70         Sink           7263.70         Sink           7263.71         Source           7264.13         Source           7264.45         Sink           7264.45         Sink           7264.45         Sink           7264.46         Sink           7264.80         Source           7264.80         Source           7265.80         Source           7265.76         Sink           7265.86	Stop acquisition           Timestamp         From         Type           720.02         DPR-120         JNFO           7262.30         Source         Native           7262.37         Sink         Native           7262.38         Source         Native           7262.73         Sink         Native           7262.73         Source         Native           7262.74         Source         Native           7262.75         Source         Native           7262.74         Source         Native           7262.75         Source         Native           7263.33         Sink         Native           7263.33         Source         Native           7263.52         Sink         Native           7263.53         Source         Native           7263.54         Source         Native           7263.90         Sink         Native           7263.91         Source         Native           7264.45         Source         Native           7264.53         Source         Native           7264.93         Source         Native      8264.95         Source         Native	Stop acquisition           Timestamp         From         Type         Details           7710.02         DPR-120         NFO         Stort HPO-High IN0-Low IN1           7726.20         Source         Native Req RD 1 bytes from 0x00000           7726.23         Source         Native Req RD 1 bytes from 0x00001           7726.23         Source         Native Req RD 1 bytes from 0x00001           7726.23         Source         Native Req RD 1 bytes from 0x00001           7726.24         Source         Native Req RD 1 bytes from 0x00001           7726.27         Source         Native Req RD 1 bytes from 0x00001           7726.27         Source         Native Req RD 1 bytes from 0x00000           7726.29         Source         Native Req RD 4 bytes from 0x00000           7726.29         Source         Native Req RD 5 bytes from 0x00000           7726.30         Sink         Native Req RD 5 bytes from 0x00000           7726.31         Source         Native Req RD 5 bytes from 0x00200           7726.32         Sink         Native Req RD 5 bytes from 0x00200           7726.31         Source         Native Req RD 1 bytes from 0x00200           7726.41         Source         Native Req RD 1 bytes from 0x00200           7726.43         Source	Stop acquisition           Timestamp         From         Type         Detals         Data           726.2.0         DR-120         INFO         Start: HPO-High INO-Low IN1         Stop acquisition           726.2.0         DR-120         INFO         Start: HPO-High INO-Low IN1         Stop acquisition           726.2.30         Source         Native Req RD 1 bytes from 0x00001         90 00 00 00           726.2.37         Sink         Native Req RD 1 bytes from 0x00011         90 01 11 100           7262.72         Source         Native Req RD 1 bytes from 0x00000         90 00 00 00 00           7262.73         Sink         Native Req RD 1 bytes from 0x00000         90 00 00 00 00 00           7263.74         Source         Native Req RD 1 bytes from 0x00000         90 00 10 00 180 018           7263.75         Source         Native Req RD 9 bytes from 0x00000         90 04 00 08         90 04 00 08           7263.75         Source         Native Req RD 9 bytes from 0x00000         90 00 00 00 00 00 00 00 00 00 00 00 00 0	Stop acquisition           Timestamp         From         Type         Details         Data           7710.02         DPR-120         NPO         Stort HPO-High INO-Low IN1         700.000         90.00.00.000         90.00.00.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.000         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72         700.72 </td

# Terminal

Terminal is a tool for running embedded DPR-120 commands.

1	Ten	minal		Sour	ce D	ULI	estir	ng															
erminal Ou	·																					lear	
DPR-120	Ref	ere	nce	511	ık																		^
help																							
dpcd_rd		dpc	d_w	r	he	elp																	
dpcd rd	0 0	x10	0																				
0x00000				01	01	01	01	81	00	00	00	00	00	00	00	00							
0x00010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x00020	00	01	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x00030	10	de	90	70	00	00	00	00	a4	b4	f9	42	00	00	00	fc							
x00040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
x00050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x00060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
x00070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
08000x0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x00090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000a0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000b0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000c0	: 00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000d0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000e0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
0x000f0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00							
																							-
	ne:																						

Currently there are three commands

Command	Description
help	List the available commands
dpcd_rd <address> <count></count></address>	Read DPCD register content. <address> is the start address; <count> is the number of register locations read. Both values are decimal by default, please use 0x prefix for hex.</count></address>
dpcd_wr <address> <value></value></address>	Write <value> to DPCD register <address>. Both values are decimal by default, please use 0x prefix for hex.</address></value>

Click Clear to clear the Terminal Output panel.

# Source DUT Testing

Source DUT Testing section is the GUI to run the compliance tests with DPR-120. Please refer to a full description about the CTS Test GUI features in chapter <u>Running</u>. <u>Compliance Tests</u> later in this document

P Input	Terminal	Source DUT Testing								
lun Tests	DUT Capab	pilities								
Test Nam	e				Pass	Fail	Skip	Timeout	Run	I
× (400.3	3. 1. 1) Succe	ssful LT at All Supported	Lane Counts and Link Speeds: HBR2 Extension		0	0	0	0	0	1
× (400.3	3.1.2) Succe	ssful LT with Request of	Higher Differential Voltage Swing During Clock R	ecovery Sequence: HBR2 Extension	0	0	0	0	0	
× (400.3	3.1.3) Succe	ssful LT to a Lower Link R	ate #1: Iterate at Max Voltage Swing: HBR2 Ex	tension	0	0	0	0	0	
× (400.3	3.1.4) Succe	ssful LT to a Lower Link R	ate #2: Iterate at Minimum Voltage Swing: HBR	2 Extension	0	0	0	0	0	
× (400.3	3.1.5) Succe	0	0	0	0	0	ľ			
× (400.3	3.1.6) Succe	ssful LT at Lower Link Ra	te Due to Loss of Symbol Lock During Channel E	ualization Sequence: HBR2 Extension	0	0	0	0	0	
× (400.3	3.1.7) Unsuc	cessful LT at Lower Link I	Rate #1: Iterate at Max Voltage Swing: HBR2 E	ctension	0	0	0	0	0	
× (400.3	3. 1.8) Unsuc	cessful LT at Lower Link I	Rate #2: Iterate at Minimum Voltage Swing: HBR	2 Extension	0	0	0	0	0	
× (400.3	3.1.9) Unsuc	cessful LT due to Failure	in Channel Equalization Sequence [loop count >	5]: HBR2 Extension	0	0	0	0	0	L
× (700.:	1. 1. 1) Additi	onal DPCD Handling Test	1		0	0	0	0	0	
× (700.:	1.1.2) Additi	onal DPCD Handling Test	2		0	0	0	0	0	
× (400.3	3.1.12) Succ	essful LT to a Lower Link	Rate #3: Iterate at Max Voltage Swing		0	0	0	0	0	
× (400.3	3.1.13) Succ	essful LT to a Lower Link	Rate #4: Iterate at Minimum Voltage Swing		0	0	0	0	0	
× (400.3	3.1.14) Succ	essful Link Downgrade to	Lowest Link Rate: Failed Clock Recovery at HBF	2, Loss of Clock Recovery during Channel Equaliz	0	0	0	0	0	
				ost Cursor during Clock Recovery & Channel Equal	0	0	0	0	0	
× (400.3	3.2.1) Succe	ssful Link Re-training Aft	er IRQ HPD Pulse Due to Loss of Symbol Lock: H	3R2 Extension	0	0	0	0	0	
× (400.3	3.2.2) Succe	ssful Link Re-training Aft	er IRQ HPD Pulse Due to Loss of Clock Recovery	Lock: HBR2 Extension	0	0	0	0	0	
🗡 (400.3	3.2.3) Succe	ssful Link Re-training Aft	er IRQ HPD Pulse Due to Loss of Inter-lane Align	ment Lock: HBR2 Extension	0	0	0	0	0	
× (400.3	3.3.1) Video	Time Stamp Generation			0	0	0	0	0	
8	Run	Test Runs: 5 🚔	Idle time between tests: 2 🚔 Seconds	Stop on Fail and Timeout				🗊 Clear	Results	;
tatus Log:										-

# 5. AUX CHANNEL MONITOR

### The AUX Tab

The tab has to dialogs. The **Transaction list** in the left displays the acquired AUX channel transactions and events. The **Message details** panel on the right side of the tab shows the parsed interpretation of the currently selected AUX channel transaction line. The **Start acquisition** / **Stop acquisition** button controls collection of the data.

ile H P Inpu	- 11 XX	Source DUT	Testing				
fain Lir	k E-EDID M	SA Log CRC		AUX			
		_					
6	Stop acquisiti	on					
Line	Timestamp	From	Type	Details	Data	Message details:	
1	5710.02	DPR-120		Start: HPD=High INO=Low IN1=		* Line #9 - 17263.01ms	
2	17262.30	Source		Reg RD 1 bytes from 0x00000	90 00 00 00	AUX ACK - 14 bytes	
3	17262.37	Sink		AUX_ACK - 1 bytes	00 12		
4	17262.53	Source		Reg RD 1 bytes from 0x00021	90 00 21 00	DPCD_REV [RO] (DPCD	revision
234567	17262.59	Sink		AUX_ACK - 1 bytes	00 01	number)	
6	17262.72	Source		Req RD 1 bytes from 0x00111	90 01 11 00	0x00000 := 0x12	5
8	17262.78	Sink		AUX_ACK - 1 bytes	00 07	DPCD V1.2	
0	17262.94	Source		Reg RD 14 bytes from 0x00000 AUX_ACK - 14 bytes	90 00 00 0d 00 12 14 c4 01 01 00 01 80 00 0		and the second second
10	17263.26	Source		Reg RD 9 bytes from 0x00400	90.04.00.08	MAX_LINK_RATE [RO] (	Maximum link
11	17263.33	Sink		AUX ACK - 9 bytes	00 00 c0 a4 44 50 52 31 32 30	rate of Main Link lanes)	-
12	17263.55	Source		Reg RD 9 bytes from 0x00500	90 05 00 08	0x00001 := 0x14	4Chor
13	17263.62	Sink		AUX_ACK - 9 bytes	00 00 c0 a4 44 50 52 31 32 30	MAX_LINK_RATE = 5.	Hopps
14	17263.81	Source		Reg RD 11 bytes from 0x00023	90 00 23 0a	MAX LANE COUNT IRO	1 (Maximum
15	17263.90	Sink		AUX_ACK - 11 bytes	00 00 00 00 00 00 00 00 00 00 0	number of lanes)	1.6-revincent
16	17264.13	Source		Reg RD 5 bytes from 0x68000	96 80 00 04	0x00002 := 0xc4	
17	17264.19	Sink		AUX_ACK - 5 bytes	00 00 00 00 00 00	MAX LANE COUNT =	4
18	17264.38	Source		Reg RD 1 bytes from 0x68028	96 80 28 00	ENHANCED FRAME C	
19	17264.45	Sink		AUX_ACK - 1 bytes	00 03	TPS3 SUPPORTED = 1	
20 21	17264.58	Source		Req WR 1 bytes to 0x02003	80 20 03 00 30		
21	17264.67	Sink		AUX_ACK - 0 bytes	00	MAX_DOWNSPREAD [RC	2]
22 23	17264.80	Source		Req RD 1 bytes from 0x00111	90 01 11 00	0x00003 := 0x01	
23	17264.86	Source		AUX_ACK - 1 bytes	00 07 90 00 30 0f	MAX_DOWNSPREAD =	: 0.5%
29	17265.09	Source		Req RD 16 bytes from 0x00030 AUX ACK - 16 bytes	00 a4 07 55 81 de 82 e5 11 b8 5		10000000000
25	17265.38	Source		Reg WR 5 bytes to 0x01000	80 10 00 04 10 02 cb 01 d5	NO_AUX_HANDSHAKE_L	.INK_TRAINI
27	17265.38	Source Trace		DOWN REO - REO: LINK ADDR	10 02 cb 01 d5	NG = 0	
28	17265.76	Sink		AUX_DEFER - 0 bytes	20	NORP [RO] (Number of I	Deceiver
29	17265.86	Source		Reg WR 5 bytes to 0x01000	80 10 00 04 10 02 cb 01 d5	North [Ko] (number of i	tecover .
30 31	17265.86	Source Trace Sink		DOWN_REQ - REQ: LINK_ADDR AUX_ACK - 0 bytes	10 02 cb 01 d5 00	DPCD Decoder mode:	
	1/265.98	allik	Nauve	n		*	
				III		1.2 + DETAILED_CAP_IN	IPO_AVAIL = •
		1	_				
De	-assert HPD	TP	ulse HPD	Pulse Duration: 1000 🚔 n	s Thort Pulse HPD		

### Decoding the Data

The AUX Monitor is compatible with both DisplayPort<sup>TM</sup> versions 1.1b and 1.2. With **DPCD Decoder mode** in the lower right hand corner of the dialog you can select which version is used and how the messages will be decoded.

The options are

- DPCD 1.1 Decoder
- DPCD 1.2 Decoder DETAILED\_CAP\_INFO\_AVAILBLE bit set =1
- DPCD 1.2 Decoder DETAILED\_CAP\_INFO\_AVAILBLE bit set =0

# Inspecting the Acquired Data

### Data Lines

The data is organized in lines, each numbered starting from 1 and marked with a timestamp. There are five kinds of data:

#### Information

Identified by the text "INFO" in their Type column, they provide some useful information like the time acquisition has started and stopped or the logical state of the inputs, etc.

#### **Transactions**

Identified by the text "Native" or "I2C" in their Type column, they report an AUX channel data transfer, either a data Request or a data Reply.

#### **Events**

Identified by the text "Event" in their Type column, they signal the state change in one or more of the monitored inputs.

#### Sideband Channel Messages

The Isochronous Transport Service uses the sideband communications over sideband channel (AUX CH and HPD) for the management of topology/virtual channel connection/Main Link and performs Main Link symbol mapping.

#### <u>Error</u>

A line Type reading "Error" marks the detection of an illegal AUX channel data packet. An irregular start condition, an irregular stop condition or transfer of a number of bits which is not a multiple of 8 are all conditions that cause an error line.

### Columns

The data on each line is ordered in columns. Each column provides additional information about the data, facilitating its viewing and interpretation:

#### <u>Line</u>

This column displays the line number, starting from 1, and cannot be hidden.

#### <u>Timestamp</u>

Each line is identified by its timestamp, marking the instant when an event or error was detected, or when a data transaction got started. The timestamp can be displayed as a time delay from the start of the acquisition (absolute) or from the previous line (relative). The timestamp can be displayed in milliseconds or in minutes, seconds and microseconds.

#### <u>From</u>

This column indicates the originator of the data line:

- "Source" and "Sink" for an AUX channel transaction, respectively a data Request and a data Reply.
- "Source Trace" and "Sink Trace" respectively for Sideband Message data Request and Reply.
- "DPR-120" for error and information lines.
- "Unknown" for signal state change events.

#### Туре

This column provides additional information about the type of the line:

- "Native" marks Native AUX channel Requests and Replies.
- "I2C" marks I2C AUX channel Requests and Replies.
- "Sideband Request" and "Sideband Reply" to mark the Sideband Channel messages
- "Event" is used for signal state change events.
- "INFO" is used with information lines.
- "Error" is used for illegal conditions detected on the AUX channel.

#### **Details**

This column contains a condensed description of the line content.

#### Data

The binary data exchanged during AUX channel transactions, in hexadecimal notation.

### Message Details

The *Message details* panel is used to provide a detailed, parsed explanation of the line currently selected in the *Transaction list*. For AUX channel transaction data, for each of the DPCD memory locations affected, the panel lists:

- All data bytes read or written.
- All DPCD memory locations affected.
- The name of the locations and of each of their bit fields.
- All bit field's numeric and binary values, together with their decoded value.
- The Replies outcome (AUX\_ACK, AUX\_NACK, I2C\_DEFER, etc.).

### Selecting Columns in the Transaction List

You can customize the *Transaction list* by clicking the right button of your mouse over the list. From the pop-up menu, you can choose which columns to display in the list.

5	271876.51 271876.70	Sink Source	Nativ Nativ	e Al	JX_ACK - 11 bytes	000	00 00 00 00 00 00 00 00 00 00 00 0 -96 80 00 04		
7	271876.77	Sink	Nat		Timestamp	•	00 00 00 00 00 00		
3	271876.90 271876.99	Source Sink	Nat Nat	✓	From		96 80 28 00 00 03		
þ	271877.09 271877.18	Source Sink	Nat Nat	✓	Туре		30 20 03 00 30 00		
2	271877.28	Source	Nat	$\checkmark$	Details		90 01 11 00		
8	271877.34	Sink	Nat	-	-		00 07		
ł.,	271877.47	Source	Nat	$\checkmark$	Data		90 00 30 Of		
5	271877.54	Sink	Nat				00 a4 07 55 81 de 82 e5 11 b8 5		
j	271877.79	Source	Nat		Filters	<b>-</b>	30 10 00 04 10 02 cb 01 d5		
	271877.79	Source Trace	Side				10 02 cb 01 d5		
	271878.18	Sink	Nat		Autoscroll		20		
	271878.27	Source	Nat		Autoscioli		30 10 00 04 10 02 cb 01 d5		
	271878.27	Source Trace	Side		Fonts & Colors		10 02 cb 01 d5		
	271878.37	Sink	Nat				00	-	DPCD Decoder mode:
		-			Refresh	F5		-	1.2 + DETAILED CAP INFO AVAIL = -
					Refresh	r0	• •		THE PERMICE ON THE OWNER

### Selecting Font and Colors of the Transaction List

Click the right button of your mouse over the transaction list, and in the pop-up menu, click **Fonts & Colors ...** to open the *Options* dialog. In the dialog click **Select new font. Y**ou can now select the font style, color and size used for displaying the *Transaction list* and the *Message details*.

### Coloring DPCD Address Ranges

In order to improve the readability of the *Transaction list*, you can mark the AUX channel transactions where a certain DPCD register address or address range is accessed with a color of your choice.

Click the right button of your mouse over the transaction list, and in the pop-up menu, click **Fonts & Colors** ... to open the *Options* dialog. In the lower part of the dialog click **Add** ... to open the *New range* dialog.

Options 🗾
Graphics options
Select new font Current font "Tahoma", size 10
Default font color
Default background color
Selected item font color
Selected item background color
Hilighted item font color
Hilighted item background color
Sideband Request Message font color
Sideband Request Message background color
Sideband Reply Message font color
Sideband Reply Message background color
Signal state change font color
Signal state change background color
Colored address ranges:
Rule #0 - RD/WR from 00050 to 00050 Rule #1 - RD/WR from 00102 to 00106 Rule #2 - RD/WR from 00202 to 00207
Background Color:
Add Edit Remove Up Down
Cancel 🖌 Cancel

In the New range dialog select the access type, start address and end address of the range that you want to be colored. Click **Accept**.

New range	411, 511, Friday	×
Any access 👻	Starting from addr. (hex)	to addr. (Hex)
Any access		
Read access	X Cance	Accept
Write access		

Select the range you just created from the Colored addresses ranges list and click the **Font Color** and **Background Color** buttons to select the colors desired.

You can create multiple simultaneous coloring rules to help you get a better at-a-glance view of the data captured. Please see an example on the next page.

Eile He	1				
DP Input	Termina	Source D	UT Testing		
Main Link	E-EDID	MSA Log CF	C Log DPCD	AUX	
_					
3	Start acqui	sition			
Line	Timestamp	From	Type	Details	Options
	118894.88	Sink		AUX_DEFER - 0 bytes	2 Graphics options
	118894.94	Source		Reg WR 5 bytes to 0x00102	
	118895.07	Sink		AUX_ACK - 0 bytes	0 Select new font Current font "Tahoma", size 10
	118895.20	Source		Req RD 1 bytes from 0x0000e	90
	118895.26	Sink		AUX_ACK - 1 bytes	0 Default font color
	118895.52 118895.58	Source Sink		Reg RD 6 bytes from 0x00202	
	118895.81	Source		AUX_ACK - 6 bytes Reg WR 4 bytes to 0x00103	0 Default background color
	118895.81	Source		AUX DEFER - 0 bytes	
	118896.19	Source		Reg WR 4 bytes to 0x00103	2 Selected item font color
	118896.38	Sink		AUX_ACK - 0 bytes	0 Selected item background color
	118896.51	Source		Reg RD 1 bytes from 0x0000e	0 Selected item background color
	118896.61	Sink		AUX ACK - 1 bytes	0 Hilighted item font color
	118896.83	Source		Reg RD 6 bytes from 0x00202	
	118896.90	Sink		AUX ACK - 6 bytes	Hilighted item background color
	118897,12	Source		Reg WR 5 bytes to 0x00102	8
	118897.47	Sink		AUX_ACK - 0 bytes	Sideband Request Message font color
	118897.60	Source		Reg RD 1 bytes from 0x0000e	01 Sideband Request Message font color
543	118897.70	Sink		AUX ACK - 1 bytes	Sideband Request Message background color
	118898.21	Source		Reg RD 6 bytes from 0x00202	9
545	118898.30			AUX ACK - 6 bytes	Sideband Reply Message font color
546	118898.46	Source	Native	Reg WR 1 bytes to 0x00102	Sideband Reply Message background color
547	118898.56	Sink	Native	AUX_ACK - 0 bytes	Sideband Reply Message background color
	118898.85	Source		Reg WR 1 bytes to 0x002c0	Signal state change font color
	118898.94	Sink		AUX_ACK - 0 bytes	
	118899.07	Source		Req WR 1 bytes to 0x001c0	80 Signal state change background color
	118899.14	Sink		AUX_ACK - 0 bytes	oq
	118899.26	Source		Req WR 1 bytes to 0x001c1	
	118899.36	Sink		AUX_ACK - 0 bytes	00 Rule #0 - RD/WR from 00050 to 00050 Font Color:
	118899.49	Source		Req WR 1 bytes to 0x001c2	0 Dula #1 DDMD From 00102 to 00105
	118899.55	Sink	Native	AUX_ACK - 0 bytes	01 Rule #1 - RD/WR from 00102 to 00106
4					
-					Background Color:
-	and a state of the		Dulas (JDC	Dutra Duration 1000	
De-a	assert HPD		Pulse HPD	Pulse Duration: 1000	
-					
					Add Edit Remove Up Down

### Searching for Data in the Transaction List

You can search and highlight lines in the *Transaction list* representing access to a selected DPCD location. Press Ctrl + F to open the search dialog and select the access type and the DPCD location address that you want to search.

The first occurrence of the found access is selected and the rest are highlighted.

	Se	ar	ch 💌
Search for	Any access	¥	to addr. (Hex):
	Any access Read access Write access		Q Search

You can use the same search criteria and search again by pressing F3.

### Filtering Data in the Transaction List

By right-clicking on the dialog and selecting **Filters** you can set up rules describing which data lines are shown in the Transaction List. You can choose the data based on:

- The type of data line
- The origin of the message
- The DPCD address range

In the *Filters* drop down menu you can find by default a set of pre-programmed filters.

2 3 4 5 6 7 8 9 10 11 12	88936.16 88936.26 88936.32 88936.38 88936.45 88936.51 88936.51 88936.67 88936.77 88936.83 88936.90 88936.96	Source Sink Source Sink Source Sink Source Sink Source Sink Source	Native Reg RD 1 bytes 1 Native AUX_ACK		90 00 0e 00	010	0 0 1 80 00 0
13	88937.06	Sink	Native AUX_ACK	Filters	•		Custom Filters
14	88937.09	Source	Native Reg WR 1	r neers			Custom miles in
15	88937.18	Sink	Native AUX_ACK				CI 110 CD
16	88937.25	Source	Native Reg WR 1	Autoscroll			Show HDCP
17	88937.34	Sink	Native AUX_ACK	Fonts & Color	re l		Hide Native
18	88937.38	Source	Native Reg WR 5	101103 02 00101			
19	88937.79	Sink	Native AUX_DEFE	Defeast	F5		Hide I2C
20	88937.86	Source	Native Reg WR 5	Refresh	61		10.1 5
21	88937.95	Sink	Native AUX_ACK - 0 byt		00		Hide Events
22	88938.05	Source	Native Req RD 2 bytes f		90 02 02 01		Hide Errors
23	88938.14	Sink	Native AUX_ACK - 2 byt		00 00 00		
24	88938.21	Source	Native Req RD 2 bytes f		90 02 06 01		Show Sideband messages only
25	88938.27	Sink	Native AUX_ACK - 2 byt		00 44 44 l		
26	88938.37	Source	Native Req WR 4 bytes		80 01 03 03 08	B 08 0	08 08
70	88038 75	Sink	Native ALIV DEEED _ 0 H	wtee	20		

The *Custom Filter* dialog provides you a possibility to add and modify new filters. The pre-programmed filters are listed in the dialog. You can copy their structure as bases of your custom filters. It is advisable not to modify the pre-programmed filters

				Custor	n Filter	X
Stor	ed custo	m filter defin	itions			
	w HDCP Native					New definition
Hide	I2C					Rename selected
Hide	Events Errors					Delete selected
Sho	w Sidebar	nd messages	; only			Move Up
						Move Down
	er Rules	oly Pairing mo	ode Auto-	- Filter item hv re	quest if reply received within 40	0us of request →
A	Rule	Type	Source	Range	Comment	opp of request
✓	Hide	Event	Any (*)	*	Hide Events	
•	Hide	Other	Any (*)	*	Hide generic or unknow	wn items
Ac	id	Edit	Remove	Up	Iown	

directly but make copies of them.

In the *Stored custom filter* definitions panel you will have the list of currently defined Filters. On the right hand side buttons you can define new Filters, rename or delete them. You can also reorder their appearance in the *Filters* pull-down menu.

In the *Filter Rules* panel lower in the dialog you can review and change the *Rules* in the selected *Filter*. By clicking **Add...** you can create new rules, clicking **Edit...** you can review and edit existing Filters and by clicking **Remove** from the Filter definition.



When you click Add... or Edit... *Edit Filter Rule* dialog opens. In the dialog you can in detail define the action of the rule, select the event and the event details.

You can get help by clicking **Help**. The "Help" text is attached to Appendix C of this document.

<i>///</i>		Edit Filter Rule	- 🗆 🗾	×
Hide	✓ Event ✓	From Any (*)	V Range: *	
Filter by	Data:			
				$\cap$
				<ul><li></li><li></li></ul>
Comment (C	Optional, max 120 chars): Hi	ide Events		

# Note Please note that Filters are a very powerful tool. They can however unintentionally hide valuable data from you. Please be careful when applying custom filters. A good practice is to start from an existing filter and gradually add new rules while testing their performance.

Note	Filtering and selecting the columns for display do not affect the actual data
	acquisition. All transactions and their full data are always captured.

### Saving Recorded Data

After the acquisition is stopped, the data displayed in the *Transaction list* can be saved as a binary file or as a report in a readable HTML or CSV format. In its binary form, the saved data can only be opened by the *AUX Monitor* feature of DPR-120 or by using Unigraf *DPA-400 GUI*. The HTML format can be opened with any available HTML browser, the CSV (Comma Separated Values) format can be opened with various text editing and spreadsheet tools.

#### Saving to a Binary File

From the top pull down menu select **File -> AUX Log as ...** and specify the name for the file to be saved. You can reload a previously saved file for later inspection using **File -> Open AUX Log ...** 

#### Creating a Test Report

The *AUX Monitor* includes a report generator that creates a test report of the results displayed in the Results Grid.

The report generated by the GUI application includes all the lines from the *Transaction list* and the content of the *Message details* panel for each of them. You can also include detailed description of the monitored source and sink and the used TE in the report.

For creating a report select from the pull down menu **File -> Save AUX Report as ...**. You can choose either a HTML or CSV format.

After selecting the report file name, in the *Report Information* dialog you can add a description of the monitored source and sink devices, and your personal remarks that will be included in the report.

🕖 Report Information							
Version Information							
Unigraf DPR-120 DTC (	GUI version: V1.10 [R0]						
DPR-120 Firmware pac [F1.3.0_N1.2.1_A1.2.							
Report Options							
Start from first line	🔘 Start at line:						
End to last line	🗇 End at line:						
CSV Separator: ;	Separate data bytes						
Source and Sink inform	nation						
Source device name:	Source 1						
Source device details:	XXXXX						
Sink device name:	Sink 2						
Sink device details:	уууу						
Remarks							
Report generated on 5.11.2015 12:35:34							
	Cancel						

Save the report by clicking **Accept** or return to the main window without saving by clicking **Cancel**. After the report is saved, your default internet browser will be opened to display the report file created.

The information entered in the dialog fields will be available also for the following reports until the GUI is closed.

Note	You can create reports from previously acquired data that has been saved in binary format. Use first <b>File -&gt; Open AUX Log</b> and then <b>File &gt; Save AUX Report as</b>
Note	Report creation for large amounts of acquired data can generate large HTML files and take several minutes. During this operation the GUI will not respond to user commands. Please, be patient.

# 6. RUNNING COMPLIANCE TESTS

DP Link Layer CTS test capability is a separate add on to DPR-120 Debug and Test Controller GUI. The tests are included in the GUI, all you need to have is the license code to enable them.

In order to get details of the content of each individual *CTS Test Product* please refer to document <u>Guide to Unigraf DP CTS Tool Options</u>. If you have any additional questions, please contact Unigraf or your local representative.

### **DUT** Capabilities

Before running the tests you have to define the capabilities of the Source DUT for the test engine. This is done in **Source DUT Testing > DUT Capabilities** tab.

🥏 Unigraf DP Debug and Test Controller							
File Help							
DP Input Terminal Source DUT Testing Run Tests DUT Capabilities							
DUT Capabilities	Time-stamp generation						
Max lanes supported:	1 Lane 2 Lanes	4 Lanes					
Max bit rate supported: HBR2 (5.4 Gbps) 💌	RBR 640x480@60 Hz 1280x720@60 Hz	▼ 1920×1080@60 Hz ▼					
HPD Unplug timeout (milliseconds): 700	HBR 1280x720@60 Hz 1280x960@60 Hz	▼ 1920x1440@60 Hz ▼					
	HBR2 1280x960@60 Hz  1920x1080@60 Hz	▼ 1920×1080@120 Hz ▼					
Video format change without LT supported	Most Packed Timings						
Link count reduction without LT supported     Driver level 3 (1.2V) supported	1 Lane 1280x800 @ 60Hz 18bpp	•					
Pre-Emphasis level 3 (9.5dB) supported	2 Lanes 1280x1024 @ 60Hz 24bpp	1280x1024 @ 60Hz 24bpp					
Fixed timing DUT	4 Lanes 2048x1536 @ 60Hz 24bpp	•					
Spread Spectrum Supported	Colorimetry						
E-DDC	RGB YCbCr 4:2:2	YCbCr 4:4:4					
	✓ 18bpp VESA 24bpp CEA (ITU.601)	24bpp CEA (ITU.601)					
Test Automation	24bpp VESA 30bpp CEA (ITU.601)	30bpp CEA (ITU.601)					
TEST_LINK_TRAINING		24bpp CEA (ITU. 709)					
TEST_VIDEO_PATTERN		30bpp CEA (ITU. 709)					
TEST_EDID_READ	30bpp CEA						
TEST_AUDIO_PATTERN	Select All						
TEST_STEREO_3D							
Event indicating DUT ready: Active Video							

The capabilities listed on the tab are explained in detail in chapter 3 Compliance Test Operation of document VESA® DisplayPort® Link Layer Compliance Test Specification: Extension Set 1.

Note Please make sure that the capability tables are completed before running the tests. The result of the test might be misleading if the DUT capabilities and the table do not match.

> You can save the settings stored in the *DUT Capabilities* tab by selecting **File > Save CTS Settings ...** You can retrieve saved settings by selecting **File > Open CTS Settings ...**

### **Running CTS Tests**

The **Source DUT Testing > Run Tests** tab lists the tests enabled with the *CTS Test Product* enabled in your Debug and Test Controller (DTC) GUI. The test name and the reference number refer to the applicable *VESA*® *DisplayPort*® *Link Layer Compliance Test Specification*. The GUI and the related FW on DPR-120 implement the test according to the specification in question. Please refer to the VESA Specification for detailed description of the procedure of the test.

For running a test, select the test with your mouse and click **Run**. For selecting multiple tests hold down the **Shift** key of your keyboard while selecting the tests.

O Unigraf DP Debug and Test Controller					•	×
File Help						
DP Input Terminal Source DUT Testing						
Run Tests DUT Capabilities						_
Test Name	Pass	Fail	Skip	Timeout	Run	^
★ (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	0	0	0	0	0	
★ (400.3.1.2) Successful LT with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 Extension	0	0	0	0	0	
★ (400.3.1.3) Successful LT to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0	
★ (400.3.1.4) Successful LT to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0	-
★ (400.3.1.5) Successful LT with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalization Sequence	0	0	0	0	0	=
★ (400.3.1.6) Successful LT at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2 Extension	0	0	0	0	0	
★ (400.3.1.7) Unsuccessful LT at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0	
✗ (400.3.1.8) Unsuccessful LT at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0	
★ (400.3.1.9) Unsuccessful LT due to Failure in Channel Equalization Sequence [loop count > 5]: HBR2 Extension	0	0	0	0	0	
X (700.1.1.1) Additional DPCD Handling Test 1	0	0	0	0	0	
★ (700.1.1.2) Additional DPCD Handling Test 2	0	0	0	0	0	
★ (400.3.1.12) Successful LT to a Lower Link Rate #3: Iterate at Max Voltage Swing	0	0	0	0	0	
★ (400.3.1.13) Successful LT to a Lower Link Rate #4: Iterate at Minimum Voltage Swing	0	0	0	0	0	
🗡 (400.3.1.14) Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery during Channel Equaliz		0	0	0	0	
🗡 (400.3.1.15) Successful LT with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Recovery & Channel Equal	0	0	0	0	0	
★ (400.3.2.1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3.2.2) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3.2.3) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-Iane Alignment Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3.3.1) Video Time Stamp Generation	0	0	0	0	0	-
🖉 Run Test Runs: 5 🚊 Idle time between tests: 2 🦉 Seconds. 🔲 Stop on Fail and Timeout				Clear	Results	
Status Log:						
						^
						-
4						

Below the list of tests you can select how many times the selected tests are performed and the time between the tests. When repeating a sequence of tests, all selected tests are performed in each repetition. E.g. when you repeat tests 1, 2 and 3 two times, the sequence is: 1, 2, 3, 1, 2, 3.

If the DUT needs time to recover after the completion of the test, you can include a pause after a test is completed and before the start of the next test. This is done in **Idle time between tests** field. The minimum time is 2 seconds.

If you have programmed a series of test to be run, you might want to stop the execution if a failure or timeout occurs. Please check the **Stop on fail and Timeout** box.

For clearing the Status Log and the Results matrix, click Clear Results.

### **Evaluating CTS Test Results**

The test procedure advancement is defined in the *Status Log* panel. It describes the steps of each individual test in the way defined in the corresponding VESA Compliance Test Specification. Please use the Status Log and the Specification side by side when interpreting the results.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

P Input Terminal   Source DUT Testing   Run Tests DUT: Capabilities						
Test Name	Pass	Fail	Skip	Timeout	Run	1
✓ (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	0	0	0	0	0	ſ
(400.3.1.1) Successful LT with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 Extension	0	0	0	0	0	Ľ
(400.3.1.2) Successful LT to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0	l
(400.3.1.4) Successful LT to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	ō	0	0	l
(400.3.1.5) Successful LT with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalization Sequence		ő	õ	0	ő	Ľ
400.3.1.6) Successful LT at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2 Extension	õ	ő	ō	0	ő	l
(400.3.1.7) Unsuccessful LT at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	ő	ő	0	0	ő	-
(400.3.1.8) Unsuccessful LT at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0	1
(400.3.1.9) Unsuccessful LT due to Failure in Channel Equalization Sequence [loop count > 5]: HBR2 Extension	õ	õ	õ	õ	õ	I
X (700, 1, 1, 1) Additional DPCD Handling Test 1	0	0	0	0	0	I
(700, 1, 1, 2) Additional DPCD Handling Test 2	õ	õ	õ	0	õ	I
✓ (400.3.1.12) Additional b) CB Handling (Cat 2) ✓ (400.3.1.12) Successful LT to a Lower Link Rate #3: Iterate at Max Voltage Swing				0	õ	I
✓ (400.3.1.12) Successful LT to a Lower Link Rate #3. Terate at Minimum Voltage Swing			0	0	0	I
(dots) 11(5) Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery during Ch				0	0	
★ (400.3.1.15) Successful LT with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Recovery &				0	0	
✓ (400.3.2.1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension				0	0	
★ (400.3.2.2) Successful Link Re-training After IRO HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3.2.3) Successful Link Re-training After IRO HPD Pulse Due to Loss of Inter-lane Alignment Lock: HBR2 Extension	0	0	0	0	0	
× (400.3.3.1) Video Time Stamp Generation	0	0	0	0	0	
(4.2.1.1) Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	1	0	0	0	1	
★ (4.2.1.2) Source Retry on Invalid Reply During AUX Read after HPD Plug Event	0	0	0	0	0	
X (4.2.2.1) EDID Read upon HPD Plug Event	0	0	0	0	0	
✗ (4.2.2.2) DPCD Receiver Capability Read upon HPD Plug Event	0	0	0	0	0	
Run Test Runs: 5 A Idle time between tests: 2 Seconds. Stop on Fail and Timeout				🗊 Clear i	Results	;
atus Log:						
Starting test: 4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event						
et MAX LINK RATE = 14h, MAX LANE COUNT = 4						
Long HPD Pulse (700 ms)						

### Creating a CTS Test Report

You can save the test results as a report in HTML format. Select **File > Save Report** ... A dialog will open where you can insert information about the DUT and remarks about the test. Details of the used test equipment and the software and firmware version will be added automatically.

Report information	
DPR-120 Serial number: 0000C001 Firmware package:	DUT Information Model: AAA Serial Number:
Firmware package Version 1.5 [F1.3.0_N0.0.17_A0.0.21_V1.1.4] Application Version V1.5 [Dec 17 2013]	123 Revision: aaa Firmware version: 1.2.3 Driver: 3.2.1
Report Information	
Tested by: N.N Remarks: (1024 chars max.)	on 2. toukokuu ta 2013
This is a test	Save X Cancel

### Viewing the CTS Test Report

The report file can be viewed with any HTML browser. The report has built-in views for Report Summary, Test Summary, view of individual tests and view of all information.

C In file///C/Users/:/Desktop/temp.htm      CUTS_TEST_STEREC.30 Event indicating DUT ready = Link Training end.      STDETAILS, TEST1      (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension      Test Result: PASSED      Test Settings:     DUT Capabilities:     Max Lanes = 4 Lanes, Max Link Rate = HBR2 (5 4 Gbps)HPD Unplug timeout: 700 ms      Test automation:     LICTS_TEST_PATTERN     LICTS_TEST_TIMING     LICTS_TEST_TEREC.30 Event indicating DUT ready = Link Training end.      Test Log      Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension.      Set MAX_LINK RATE = 08h, MAX_LANE_COUNT = 1	DPR-120 CTS Test Report ×	
LLCTS_TEST_STEREC_3D Event indicating DUT ready = Link Training end. <b>STDETALLS, TEST 1</b> (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension Test Result PASSED Test Settings: DUT Capabilities: Max Lanes = 4 Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout: 700 ms Test automation: LLCTS_TEST_UNK_TRAINING LLCTS_TEST_PATTERN LLCTS_TEST_PATTERN LLCTS_TEST_TRAINING LLCTS_TEST_TRAINING LLCTS_TEST_TRAINING LLCTS_TEST_TRAINING Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension. Set LOG Starting Test: (400.31.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension. Set MAX_LINK_RATE = 08h, MAX_LANE_COUNT = 1 Long HPD Pulse (200 ms) Wat until Succe DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields Source DUT writes TRAINING_PATTERN_SET = 1h Source DUT writes TRAINING_PATTERN_SET = 1h CR LICK succeeded on all active lanes Source DUT writes TRAINING_PATTERN_SET = 3h	C I file:///C:/Users/-/Desktop/temp.htm	
(400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension Test Result: PASSED Test Settings: DUT Capabilities: Max Lanes = 4 Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout: 700 ms Test automation: LICTS_TEST_LINK_TRAINING LICTS_TEST_PATTERN LICTS_TEST_PATTERN LICTS_TEST_TAUDIO_PATTERN LICTS_TEST_TAUDIO_PATTERN LICTS_TEST_TAUDIO_PATTERN LICTS_TEST_TIMING Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension. Set MAX_LINK_RATE = 08h, MAX_LANE_COUNT = 1 Long HPD Pulse (200 ms) Wat until Source DJT writes to the LINK_BW_SET and LANE_COUNT_SET fields Source DJT writes times to the LINK_BW_SET and LANE_COUNT_SET fields Source DJT writes TRAINING_PATTERN_SET = 1h CR LICK succeeded on all active lanes CR Lick succeeded on all active lanes Source DJT writes TRAINING_PATTERN_SET = 3h	LLCTS_TEST_STEREO_3D	
Test Result: PASSED Test Settings: DUT Capabilities: Max Lanes = 4 Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout: 700 ms Test automation: LLCTS_TEST_LINK_TRAINING LLCTS_TEST_PATTERN LLCTS_TEST_PATTERN LLCTS_TEST_PATTERN LLCTS_TEST_PATTERN LLCTS_TEST_STERAE3D Event indicating DUT ready = Link Training end. Test Log Starting Test: (400.31.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension. Set MAX_LINK_RATE = 08h, MAX_LANE_COUNT = 1 Long HPD Pulse (200 ms) Wat until Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields Source DUT writes TRAINING_PATTERN_SET = 1h	ST DETAILS, TEST 1	
Test Settings: DUT Capabilities: Max Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout: 700 ms Test automation: LICTS TEST LINK TRAINING LICTS TEST PATTERN LICTS TEST TAUDIO, PATTERN LICTS TEST TAUDIO, PATTERN LICTS TEST TIMING LICTS TEST TIMING TEST TIMING LICTS TEST TIMING LIC	(400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	
DUT Capabilities: Max Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout. 700 ms Test automation: LICTS_TEST_LINK_TRAINING LICTS_TEST_PATTERN LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TIMING LICTS_TEST_TEST_TEST_TEST LICTS_TEST_TEST_TEST_TEST LICTS_TEST_TEST_TEST_TEST_TEST LICTS_TEST_TEST_TEST_TEST_TEST_TEST_TEST_T	Test Result: PASSED	
LLCTS_TEST_LINK_TRANING LLCTS_TEST_ADTERN LLCTS_TEST_ADTERN LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TEST_TIMING LLCTS_TEST_TEST_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TES	DUT Capabilities:	
Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension.         Set MAX_LINK_RATE = 06h, MAX_LANE_COUNT = 1         Long HPD Pulse (200 ms)         Wat until Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields         Source DUT sets LINK_BW_SET = 1         Source DUT sets LINK_BW_SET = 06h         Source DUT writes TRAINING_PATTERN_SET = 1h         CR LINK_Succeded on all active lanes         Source DUT writes TRAINING_PATTERN_SET = 3h	LLCTS TEST_LINK_TRANING LLCTS_TEST_ANDIO_PATTERN LLCTS_TEST_ANDIO_PATTERN LLCTS_TEST_TIMING LLCTS_TEST_TIMING LLCTS_TEST_STEREPO_3D	
Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension. Set MAX_LINK_RATE = 06h, MAX_LANE_COUNT = 1 Long HPD Puble (200 ms) Waf until Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields Source DUT sets LANE_COUNT_SET = 1 Source DUT sets LINK_BW_SET = 06h Source DUT writes TRAINING_PATTERN_SET = 1h 		
Set MAX_LINK_RATE = 08h, MAX_LANE_COUNT = 1 Long HPD Pulse (200 ms) Wad until Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields Source DUT sets LANE_COUNT_SET = 1 Source DUT sets LINK BW_SET = 06h Source DUT writes TRAINING_PATTERN_SET = 1h CR LI fiter, 1 lanes CR LI fiter, 1 lanes CR lock succeeded on all active lanes Source DUT writes TRAINING_PATTERN_SET = 3h	Test Log	
Long HPD Pulse (200 ms)	Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension.	
Source DUT sets LANE, COUNT_SET =1 Source DUT sets LINK BW, SET = 06h Source DUT sets LINK BW, SET = 06h CR LT iter, 1 ianes CR LT ket, 1 ianes CR Ltok succeeded on all active lanes Source DUT writes TRAINING_PATTERN_SET = 3h	Long HPD Pulse (200 ms)	
CR lock succeeded on all active lanes Source DUT writes TRAINING_PATTERN_SET = 3h	Source DUT sets LANE_COUNT_SET =1 Source DUT sets LINK_BW_SET = 06h Source DUT writes TRAINING_PATTERN_SET = 1h	
	CR lock succeeded on all active lanes	
EQ LT iter1 lanes Equalization succeeded on all active lanes Symbol lock succeeded on all active lanes	EQ LT iter, 1 lanes	

# APPENDIX A. PRODUCT SPECIFICATION

# DPR-120

1	
Input	1 x DisplayPort™ HBR2 and MST compliant Rx, ST Microelectronics STDP9320 controller (DP In)
Outputs	1 x DP 1.2 multi stream Tx (DP Out)
	1 x DP 1.1 compliant preview monitor (Monitor Out)
	S/PDIF coaxial audio monitor
	TRS headset audio monitor
Resolutions	4096 x 2160 input & pass through
	2560 x 1600 preview
Audio	Up to 2 LPCM channels at 192 kHz, 24-bits or multi-channel compressed (AC3, DTS, etc) compliant with IEC60958 / IEC61937
Control	USB 2.0 interface
Software	Debug and Test Controller GUI
	Test Automation Shell (option)
	DP RefSink CTS LL Extensions (option)
Power supply	AC/DC Power supply
	(100 to 240 Vac 50/60 Hz input, +5 Vdc output)
Mechanical Size	230 x 168 x 56 mm
Weight	0.9 kg w/o power supply

All specifications are subject to change without notice.

# APPENDIX B: TEST AUTOMATION SHELL

Test Automation Shell (TA Shell) is a license enabled optional feature for DPR-120. It enables the user to create simple automated test routines. All functions that are in the DTC GUI can also be accessed through the TA Shell.

🗈 DPR-120 Shell, V1.9 [R0], (C) 2014, Unigraf Oy. All Rights Reserved.
DPR-120 Shell, U1.9 [R0], (C) 2014, Unigraf Oy. All Rights Reserved. Entering interactive mode Enter 'HELP' for instructions.
Base > open 1 Searching devices 1 Devices found: - Device ID [1]: DPR-120 [1350C369], Serial 1350C369
Device DPR-120 [1350C369] Opened. Device version: Firmware package Version 1.9 [F1.3.0_N1.2.0_A1.2.0_V1.1.4]
Loaded 2 liconses. DPR-120 [1350C369] > DPIN Status Clock Recovery [XX] [XX] [XX] [XX] Symbol Lock [XX] [XX] [XX] [XX] Channel equalization [XX] [XX] [XX] Voltage Swing (mUpp) 400 400 400 400 Pre-Emphasis (4B) 3.5 3.5 3.5 3.5 LaneCount = 4 FrameMode = Enhanced MST = Enabled Linkrate = HBR2 Scrambling = Enabled DPR-120 [1359C369] > _

Please find below a quick list of TA Shell commands. For full description of each command, please refer to *Shell\_User\_Manual.pdf* included in the DPR-120 Release Package.

```
Help <topic> [...]
Exit
Open <Device ID>
List
Close
CLS
Run <DOS Command>
License add <key>
License list
License remove <key-index>
License save
License load
DPIN HPD <Operation>
DPIN Linkconfig show
DPIN Linkconfig <Lane_count> <Speed> <MST> <TPS3>
DPIN DPCD Read <Address> [Length]
DPIN DPCD Write <Address> <Data1> [Data2]
DPIN DPCD Save <Target-file> <Address> [Length]
DPIN DPCD Load <Source-file>
DPIN Status
DPIN Streams
SINK EDID Load <Source-file>
SINK EDID Save <Target-file>
```

```
DPMON Select <Stream Index>
DPMON Read <Data_ID>
DPMON Log Start <Data ID> <Target File>
DPMON Log Stop <Data ID>
CTS List
CTS Config load <config_file>
CTS Config save <config_file>
CTS Config show [conf entry]
CTS Config Link <Max-lanes> <Max-rate> <HPD Timeout>
CTS Config flags <'+'|'-'> <Flag1> [Flag2] [...]
CTS Config ta flags <'+'|'-'> <Flag1> [Flag2] [...]
CTS Config ready_event <Event>
CTS Config timestamp <BitRate> <Lanes> <ResolutionID>
CTS Config most_packed <ResID1> <ResID2> <ResID4>
CTS Config colorimetry <'+'|'-'> <CL_ID1> [CL_ID2] [...]
CTS Run <Test_Index>
Proceed
Pass
Fail
Abort
CTS Report DUT_Model <String>
CTS Report DUT_Revision <String>
CTS Report DUT_FW <String>
CTS Report DUT Serial <String>
CTS Report DUT Driver <String>
CTS Report Tester <String>
CTS Report Remarks <String>
CTS Report show
CTS Report save <Target_File>
```