

4. FIRMWARE UPDATE PROCEDURE

FW Update Tool

The firmware (FW) of UCD-400 is programmed with a separate tool called **Quartus Prime (includes Nios II EDS)**. The tool can be downloaded from **Intel® FPGA** website:

<https://fpgasoftware.intel.com/?edition=lite>

On the download page, please **Select release 16.1**. Please download **Quartus Prime (includes Nios II EDS)**.

Quartus Prime Lite Edition
Release date: November, 2016
Latest Release: v19.1

Intel® Quartus® Prime
Design Software

Select release: 16.1 Please select release 16.1

Operating System Windows Linux

✓ A newer version of the Quartus Prime Design Software is available. Users should upgrade to the latest version of the [Quartus Prime Design Software](#). This version does not include the latest open source components that have functional and security updates. For critical support requests, please contact our [support team](#).

✓ You may be exposed to a vulnerability issue if you have installed or plan to install Quartus Prime/Quartus II software from v11.0 to v18.0 to a location with space(s) in the path. See this [KDB solution](#) for more details.

✓ The Quartus Prime Lite software version 16.1 supports the following device families: Arria II, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. [More](#)

Combined Files Individual Files Additional Software Updates

Download and install instructions: [More](#)
[Read Intel FPGA Software v16.1 Installation FAQ](#)
[Quick Start Guide](#)

Updates Available

Quartus Prime Lite Edition (Free)

Quartus Prime (includes Nios II EDS)
Size: 2.0 GB MD5: 0FFD781FCC23C6FABC6A68019B3CAB62

ModelSim-Intel FPGA Edition (includes Starter Edition)
Size: 1.1 GB MD5: F665D7016FF793E64F57B08B37487D0E
** Require 32-bit libraries, see [installation manual](#).

Devices
You must install device support for at least one device family to use the Quartus Prime software.

Arria II device support
Size: 409.6 MB MD5: 77F1518FE38765F110A904E7C6A680A7

Note: Registering is needed for the download.

Please download and install the tool in the PC.

Connect to the UCD-400 Unit

- ▶ Power on the UCD-400.
- ▶ Connect UCD-400 with a USB cable to the PC through **Programmer** connector. (Pls refer to page 7)

The programming interface is the Ethernet connector in the UCD-400 unit. The PC can be connected to the UCD-400 unit either through a network HUB or directly.

Please follow either of the two procedures below.

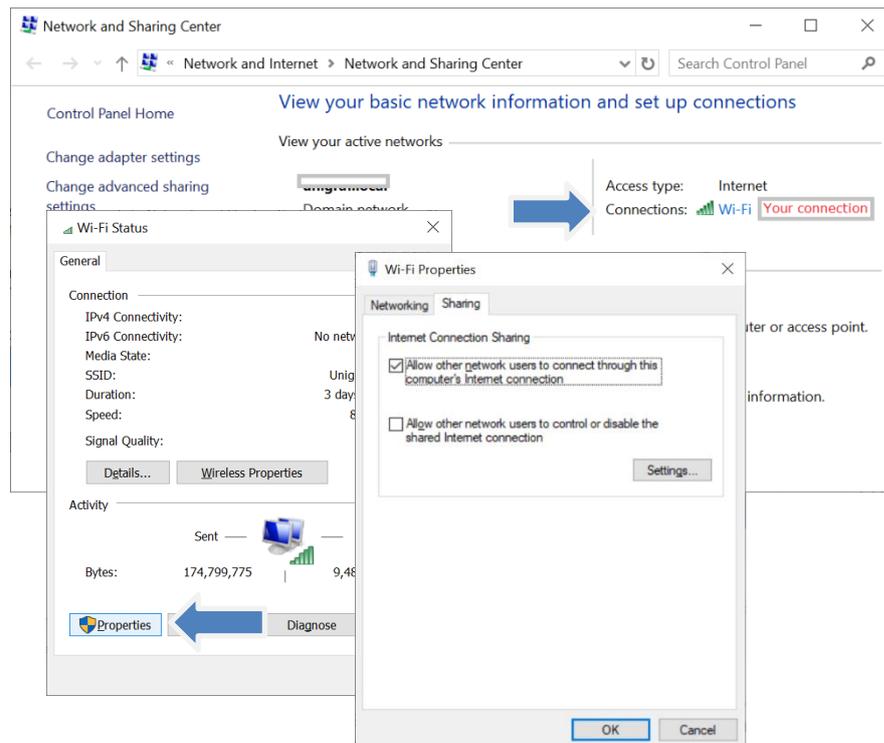
Connecting Through Ethernet Network (Alternative 1)

- ▶ Connect UCD-400 through **Ethernet** connector to the same network HUB where the programming PC is connected.

Connecting with Direct Ethernet Cable (Alternative 2)

In case of direct connection, the PC needs to be configured to be an Ethernet network host by enabling WIFI network share (The WIFI network will not be used for programming).

- ▶ Connect UCD-400 directly to the PC through **Ethernet** connector;
- ▶ Enable **WIFI** Internet access of the PC.
- ▶ From Network and Sharing Center click on the WiFi connection
- ▶ In Wi-Fi Status dialog click **Properties** and select **Sharing** tab
- ▶ Select *Allow other network users to connect through this computer's Internet connection*
- ▶ Click **OK** and **Close**.



Note The network sharing is shown above for Windows 10. Similar controls can be found for other Windows versions and other operating systems.

Programming the FW

- ▶ Run Nios II 16.1 Command Shell application as Administrator

Note	<i>Nios II 16.1 Command Shell</i> application needs to be run as Administrator (Right click with mouse and select Run as Administrator)
Hint	Right click on the top edge of <i>Command Shell</i> and select Edit > Paste to paste the commands below

- ▶ Select FW update folder location. For example:

```
cd /cygdrive/c/Program Files (x86)/Unigraf/TSI/UCD-400/Firmware/
```
- ▶ Run the boot loader that initiates the HTML programming interface.

```
source run.sh
```

Upon command completion, the assigned IP address for UCD-400 device is highlighted in the picture below.

```

/cygdrive/c/Program Files (x86)/Unigraf/TSI/UCD-400/Firmware
jsa@t440s /cygdrive/c/Program Files (x86)/Unigraf/TSI/UCD-400/Firmware
$ source run.sh
Searching for SOF file:
In :
  a10_fpga_bup.sof

Warning (210120): Arria 10 information is incomplete. The ISP clamp functionality will be disabled.
Info:
Info: Running Quartus Prime Programmer
Info: Command: quartus_pgm --no_banner --mode=jtag -o p;a10_fpga_bup.sof
Info (213045): Using programming cable "USB-BlasterII [USB-1]"
Info (213011): Using programming file a10_fpga_bup.sof with checksum 0x30E7799E for device 10ax115s3f45e2sge3@1
Info (209060): Started Programmer operation at Mon Jan 20 11:13:25 2020
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x02E6600D
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Mon Jan 20 11:13:40 2020
Info: Quartus Prime Programmer was successful. 0 errors, 1 warning
Info: Peak virtual memory: 5626 megabytes
Info: Processing ended: Mon Jan 20 11:13:40 2020
Info: Elapsed time: 00:00:29
Info: Total CPU time (on all processors): 00:00:16
Using cable "USB-BlasterII [USB-1]", device 1, instance 0x00
Pausing target processor: OK
Initializing CPU cache (if present)
OK
Downloaded 411KB in 0.4s (1027.5KB/s)
Verified OK
Waiting to allow other programs to start: done
Starting processor at address 0x102002BC
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "USB-BlasterII [USB-1]", device 1, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)

PHY INFO: [phyid] 0x0 0x141 0xcc2

PHY INFO: [phyid] 0x0 0x141 0xcc2
InterNiche Portable TCP/IP, v3.1

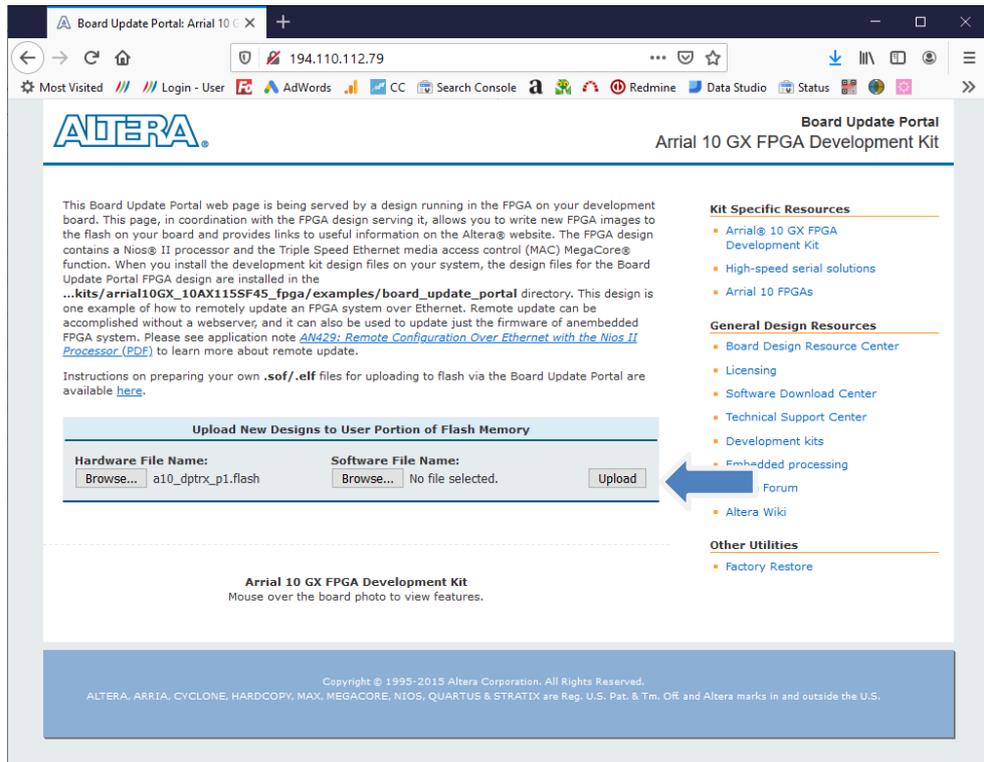
Copyright 1996-2008 by InterNiche Technologies. All rights reserved.
prep_tse_mac 0

Your Ethernet MAC address is 00:07:ed:2a:09:44
prepped 1 interface, initializing..
[tse_mac_init]
INFO : TSE MAC 0 found at address 0x10003000
INFO : PHY Marvell 88E1111 found at PHY address 0x00 of MAC Group[0]
INFO : PHY[0.0] - Automatically mapped to tse_mac_device[0]
INFO : PHY[0.0] - Restart Auto-Negotiation, checking PHY link...
INFO : PHY[0.0] - Auto-Negotiation PASSED
INFO : PCS[0.0] - Configuring PCS operating mode
INFO : PCS[0.0] - PCS SGMII mode enabled
INFO : PHY[0.0] - Checking link...
INFO : PHY[0.0] - Link established
INFO : PHY[0.0] - Speed = 1000, Duplex = Full
OK, x=0, CMD_CONFIG=0x00000000

MAC post-initialization: CMD_CONFIG=0x0400020b
[tse_sgdma_read_init] RX descriptor chain desc (1 depth) created
mctest init called
IP address of et1 : 0.0.0.0
Created "inet main" task (Prio: 2)
Created "clock tick" task (Prio: 3)
Acquired IP address via DHCP client interface: et1
IP address : 194.110.112.79
Subnet Mask: 255.255.255.0
Gateway : 194.110.112.1

```

- ▶ Launch web browser on the PC. If Ethernet connection is used, please make sure that the PC is connected to the same network as the UCD-400 unit.
- ▶ Access the HTML programming interface by entering the IP address assigned for the UCD-400 unit.



- ▶ Browse **Hardware File Name** for UCD-400 update (e.g. **a10_dptrx_p1.flash**) and then press “Upload” button
- ▶ Once uploading process done – cycle power on the UCD-400.

Note Please cycle the power on the UCD-400 unit to enable the FW update.
