UCD Console for UCD-424



User Manual



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1. ABOUT THIS MANUAL

Purpose

This guide is User Manual of UCD-424, USB-connected video interface test unit for use with a PC with Windows® 10 Windows® 8 or Windows® 7 operating system.

The purpose of this guide is to

- Provide an overview of the product and its features.
- Provide instructions for the user on how to install the software and the drivers.
- Provide instructions for the user on how to update the FW of the unit.
- Introduce the HW features of the UCD-424 units.
- Provide instructions for the user on how to use UCD Console software.

Product and Driver Version

This manual explains features found in UCD Console Software Package **1.12**. Please consult Unigraf for differences or upgrades of previous versions.

Please consult the Release Notes document in the installation package for details of the SW and FW versions and changes to previous releases.

Notes

On certain sections of the manual, when important information or notification is given, text is formatted as follows. Please read these notes carefully.

Note

This text is an important note

2. INTRODUCTION

Product Description

UCD-424 is a high speed, USB 3.0 connected video interface test unit. *UCD Console* is the common graphical user interface (GUI) for Unigraf's UCD-400 and UCD-300 family units. The outlook and details of UCD Console will be different depending on the capabilities of the connected unit reflecting the features enabled.

UCD-424 units feature a high-level Software Development Kit (SDK) for use in automated testing. It is called Test Software Interface (TSI). TSI allows for an easy integration of Production and R&D testing routines into an automated test system environment. Please refer to TSI documentation found in additional Unigraf manuals for more details.

Product Features

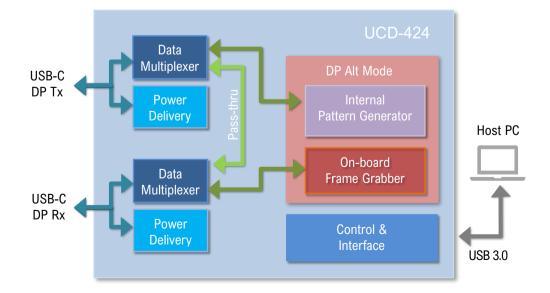
- High resolution video and audio capture up to 8K 30 Hz, 4K / UHD 120 Hz
- Supports HBR3 feature of DP 1.4a
- Compatible with HDCP versions 1.3 and 2.3
- 2 GB on-board high-speed video buffer
- High speed USB 3.0 host PC interface

Please refer to Product Specifications in the appendix of this document for details.

Functional Description

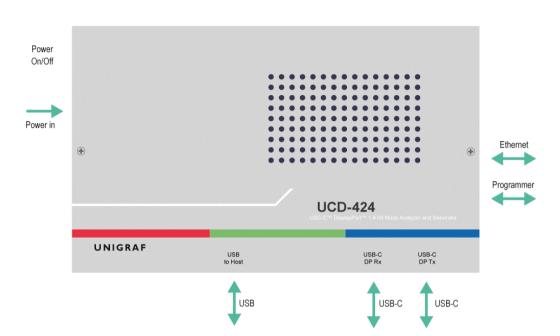
UCD-424 units consist of a multimedia signal input stage, an internal pattern generator, a control stage with on-board frame buffer and a PC interface stage. In the Input Stage the signal is conditioned and converted to desired format. The Interface and Control stages are either passing the captured data directly to the USB interface or storing it to the frame buffer. The internal pattern generator is able to source a signal for testing sink and branch units. The Interface & Control stages are receiving instructions from the host PC to configure and control the functionality of the unit.

Please find below logical diagram of UCD-424 unit.



UCD-424

The image below indicates the connections in UCD-424 unit and their description.



Name	Description
USB-C DP Tx	USB-C connection with DisplayPort™ 1.4a Alt Mode upstream Source capability
USB-C DP Rx	USB-C connection with DisplayPort™ 1.4a Alt Mode upstream Sink capability
USB	USB 3.0 connection to the host PC
Power in	+12 Vdc Power Supply Input
Power On/Off	Rocker power switch
Programmer	Optional USB interface for configuring the device FW (behind a cover) (Not used by default)
Ethernet	Optional Ethernet interface for updating the device FW (behind a cover) (Not used by default)

Note	Capturing and sourcing high resolution video modes, especially 4K and 8K video
	modes and the 120 Hz frame rate set stringent requirements on the video cables and
	connectors.

Warning In order to avoid damage to the unit and the PC, please always attach the power cord (Power In) to the unit first, and after that connect the USB cable to the PC.

Unpacking

The UCD-424 product shipment contains:

- The UCD-424 unit
- AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +12 Vdc output)
- USB 3.0 compliant cable for host PC connection
- USB-C to USB-C USB 3.2 Gen2 e-marked cable
- USB-C to DP Bi-directional Cable for testing DP sinks or sources

Installation Package

The UCD-424 software installation package can be obtained from Unigraf download page at <u>https://www.unigraf.fi/downloads/</u>.

The installation package is a bundle between the components needed for UCD Console and for TSI SDK. The bundle contains the following items:

- Windows drivers (installed during set up)
- UCD Console software GUI (installed during set up)
- License Manager (installed during set up)
- DSC Test Content and DSC compression tools (optionally installed during set up)
- TSI SDK (optionally installed during set up)
- User Manuals including this document.

In some cases, also the firmware of the unit needs to be updated. If in doubt, please contact Unigraf.

Note: The software should be installed before connecting the UCD-424 unit in the PC.

Note:

System administrator's privileges are required for performing the installation.

Software Installation

Start the installation by running **Unigraf Software Bundle Setup.exe**

Once the installer has started, a welcome page is displayed. Welcome page shows the software package release version.

Click Next to continue. In the next dialog the user needs to agree to Unigraf Software End User License and select the components installed.

Note: Please note that the size of the DSC Source Bitmap Files is 2.6 Gbytes, and that the size of the generated DSC Content Library may exceed 200 Gbytes

- Next dialogs define the installation folder in your PC and the Start Menu folder used.
 - When the selections are ready, click **Install** to start the installation.
- Click **Finish** to exit the installation dialog.

3. LICENSE MANAGER

Licensing

The features of UCD Console GUI are divided into groups based on the target use of the device. Some basic features can be used without licenses. Advanced feature groups have their dedicated licenses that open the related part of the GUI or enable the related control.

Unigraf licenses are provided as strings of characters, **License Keys**. Each License Key enables a dedicated function in one device. Each device has its dedicated **Seed Number**. Each **License Key** is tied to one **Seed Number**. License Keys can be freely used in any number of PCs

License keys are managed with Unigraf License Manager. By default, shortcut to Unigraf License Manager can be found in Start Menu.

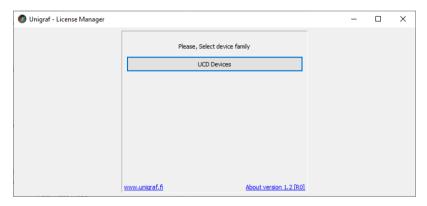
Please click **Yes** in the first dialog. License Manager can be run only with Administrator rights.

Note:

System administrator's privileges are required for accessing the licenses.

License Manager GUI

When run, License Manager will list the licensing enabled Unigraf devices. If no suitable device families are detected, License Manager will exit. Please first select one of the available device families by clicking one of the device family selector buttons.



In the list of Attached Devices please select the device in question. The *serial number* and the *seed number* of your device are printed in a sticker attached to the bottom of the device.

-			
🕖 Unigraf - License Manager	-		\times
d Back	License management for UCD-1, UCD-	2, UCD-3xx	Devices
Attached Devices:			
UCD-400 [1949C335] SW Emulated device [EMU001]	Select a device to edit licenses		

The **Back** button opens the device family selection screen. The **Refresh** button will re-scan the system for installed hardware.

Managing Licenses

Seed Number

• · · · · · · · · ·				_	
🕖 Unigraf - License Manager			-		\times
d Back		License management for UCD-1	, UCD-2	, UCD-3xx	Devices
Attached Devices:	Enter new license for device with se	ed number 70b076560100005f:			
UCD-400 [1949C335] SW Emulated device [EMU001]				Insta	ll
	Installed licenses:				
	License	Key			
	TSI Advanced Set with HDCP2.2	33MC-U 🚛 🚛 🖉 🦷 👘 👘 🖬 🛻 I5-TQYU			
	UCD Pro for DP Sink UCD Pro for DP Source	68P7-V			
	HDCP 2.2 Support	S9W6-F			
C Refresh	🔄 Import	Export	3	Remove Se	lected

Each license is tied to a hardware unit with the help of the **Seed Number**. Each unit has a unique Seed Number. Seed Number of the selected unit can be found in the top of the dialog.

Seed Number of the selected device can be copied from dialog link for e.g., ordering Licenses.

Adding New License Keys

To add a new license key for a device, please enter the characters from the license sticker to the boxes provided. The License Manager will automatically move the caret across the edit boxes during typing. If the key is given in text format, copy it and paste to the leftmost box.

Once the license key is fully entered, click the **Install**. The license is authenticated and if it is valid, the license will appear in the list of installed licenses. If the key fails to authenticate, an error message is displayed. If this happens, please make sure that the key has been typed correctly and that the seed number on the license key sticker matches the seed number displayed seed number for the device.

Please note that to avoid confusion, some letters will never appear in a license key because they resemble numbers: For example, capital 'G' and number '6' are very similar when printed with small font. When in doubt, use numbers.

Also, please notice, that characters that can't be part of valid license key are not accepted as input. When appropriate an automatic conversion is applied while typing: For example, lower case letters are converted to upper case automatically.

Managing Installed Licenses

The Installed licenses list shows all currently installed licenses for the currently selected device. The list shows the actual license key, and what that key unlocks.

Remove Selected will uninstall selected licenses. To uninstall a license, click on the license and then click the Remove Selected button.

Export will allow all installed licenses for the currently selected device to be saved into an INI file for backup and distribution to other PCs. To export a license, click on the license and then click the Export button. Please notice that licenses from multiple devices can be exported into the same INI file.

Import will install licenses from an INI file for the currently selected device.

4. FIRMWARE UPDATE

UCD Configuration Utility is used to load an updated firmware to the device.

```
Note: Firmware update is a sensitive process. Please do not disconnect the device from the PC and do not power it off before the operation is completed unless specially requested. Avoid plugging and unplugging other USB devices when the firmware update is in progress.
```

To update the firmware or create a new configuration on a UCD-424 device, please perform the following steps:

- Connect the UCD-424 unit to a power supply and connect the USB cable.
- ▶ Open UCD Console. Select Tools > Firmware update.

You can launch alternatively UCD Firmware Configuration tool in Start Menu.

UCD Configuration Utility	×
	× ///
Please clic	k Next to update your UCD device.
Available Firmware Pac	kages Included components:
Device Fin UCD-3xx 0.0	Ware UX 2.2.2 UF 1.3.4
UCD-4xx DP 0.0 UCD-4xx HDMI -	
	< Back Next > Cancel

The first page of the utility indicates the firmware component versions present in the package. Please click **Next**.

UCD Configuration Utility		×
Connected UCD Devices Please select the device		× ///
l	ICD-3xx devices	
	JCD-424 [1950C336] JCD-400 [1938C320]	
	JCD-400 [1938C320]	
Multiple UCD devic applications during	es found. Make sure not to run other Unigraf configuration.	
	< Back Next >	Cancel

From the list of connected UCD-300 devices please select the one that you want to update. Click Next.

Updated Modules

The tool indicates the firmware file to be used and prompts for selection of the firmware modules to be updated. It compares the modules in the selected device and omits the ones that are the same.

	UCD Modules Modules that should be updated are checked									
Selected de	evice: UCD-424 [19	50C336]								
Module	New	Existing	Comment							
✓ Main	3.0.4/1.9.49	3.0.6/1.9.50	Can be updated							

▶ When you are done, click **Next**.

Power Cycle

When re-initiating the firmware of a UCD device the whole process cannot be done during one session. Therefore, on certain point, user needs to **power cycle** the device (switch off the power > wait for 10 seconds > switch on the power).

Click **OK** button on the dialog.

ICD Configuration Utility		×
Configuration in progress	11	//
LICD-323 (1823C398) Par MC >>MC 0.21 26 Withing image body Erased in 257.0 seconds (2) Read from 19:5 JTS CF000203 Witten in 26.0 seconds Completed in 285.0 seconds Completed in 285.0 seconds	Attention	× Please do the following: - Power OFF the device. - Wait for 10 seconds. - Power ON the device. - Press OK when done
< Back Comple		OK

Note:

The procedure may take several minutes depending on the speed of the USB connection of the host PC.

5. UCD CONSOLE

UCD Console is the graphical user interface (GUI) of UCD-424 for desktop use. It provides the user access to all features of the unit. UCD Console also includes powerful debugging and analysis tools enabling the user to monitor the status of the display interfaces and assist in the problem detection.

The various features of the UCD-424 are divided into interface specific screens and tabs. Each tab contains data and controls for a specific feature.

Device Selection

A shortcut of UCD Console can be found by default under Start Menu. Once UCD Console GUI is launched the dialog provides a list of UCD devices connected in the PC. Please select the target device by clicking on the appropriate button. If your device cannot be found in the list, please confirm the power and USB connection to the device and click the **Rescan**... button.

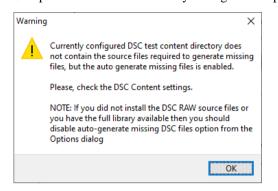
///	UCD Co	nsole				-	×
<u>F</u> ile	<u>V</u> iew	<u>T</u> ools	<u>H</u> elp				
Device							
					Select Device		
					UCD-424 [1950C336] UCD-400 [1938C320]		
					🕄 Rescan		
			Y	www.unigraf.fi	UCD Console V1.8 [R40], Build# 28026		
			_				

Select Role

The use of UCD-424 devices with UCD Console is divided in display interface specific roles. The structure of UCD Console varies between roles by having a varying set of tabs dedicated to functionalities available in the enabled role. The table below lists the roles and tabs available in each role. Please find a detailed description of each role in the later chapters of this manual.

Warning about DSC Test Content

When running DSC Compliance Tests, UCD-424 needs to have access to DSC content used as test patterns. The content can be created from the source bitmap files downloaded during installation (optional) either with Unigraf DSC Content Creator or created by the Compliance Test Tool on-the-fly during the compliance test.



If *Automatically create missing content* is selected in Tools > Options menu, but the source files have not been installed a *Warning* dialog will open. Clicking **OK** will open the *Option* menu.

You can either re-install the whole SW package with DSC Content Library or deselect *Automatically create missing content* in Option menu.

Applying Changes

In various UCD Console dialogues the user needs to update several parameter or fields to make the changes needed. In order to avoid false combinations of parameters the new parameters are applied to UCD-424 only after **Apply** is clicked. In UCD Console the situation that parameters have been changed but not applied is indicated by **bold values** of the parameter.

///	UCD-424 [1950	C336] - USB-C Source	and Sink				- 0	Х
<u>F</u> ile	<u>V</u> iew <u>T</u> ools	<u>H</u> elp						
	USB-C Patt	ern Generator Audio Ge	enerator Link (ED			nk DUT Testing	7	
8	Video Patter	n Generator					Custom image	
Device	MST	Number of streams 1	•			^		
A T T	Other 512	0 x 2880 @ 60.0Hz	✓ 10 bpc	~ Ch	essboard	\sim		
X	RGB	~	\sim	1	* 1	A V	10 M	
8			\sim 8 bpc					
Event Log	RGB	\sim	\sim	1	1 •	×	MAX	
ent			✓ 8 bpc					
L L	RGB	~	\sim	1	* 1	×	Default.bmp Click on image to load	
			8 bpc					

Options

Options can be found in **Tools > Options**.

ptions				
Video, Audio a	nd Misc options	AUX Analyze	er options	
Image File F	ormat			
PPM	(⊖ JPG	
Audio File Fo	rmat			
• WAV				
Audio Buffer	size			
Main buffer,	Ksamples	16	Playback buffer, Ksa	amples 4
Folders				
Directory to	save images ar	nd audio		
C:\Users\Te	ster\Pictures			Browse
Presets direc	tory			
				Browse
200				
DSC				
DSC Work fo				Pr
				Browse
	tent directory			9
E:\DSC_con	ent_library\			Browse
Automati	ally create mis	sing contents		
Keep (uto-created D	SC content file	s	
Misc. options				
Apply col	our conversion	to saved image	es	
Bypass 4	2:x -> 4:4:4 c	onversions		
	or is not HDCP			
TSI Integrat	on			
Enable TS	I Integration			
	-	ownerted D/ 77 -	est to 'RunTest' scri	at
				pt
Always a	ppena when e	xporting to a n	ew file	~
		•	ГОК	🗙 Cancel

Video Audio and Misc. Options

Image File Format

You can save the captured frames either in PPM, BMP or JPG bitmap file format. In PPM format the files are stored with the captured color depth, with other formats the color depth is truncated to 8 bits per color.

Audio File Format

Audio files are stored in WAV format

Audio Buffer size

Main buffer: Length of the buffer in the PC memory storing audio samples for monitoring audio format in DP RX / Audio tab. Increased buffer length will enable longer time span to be monitored.

Playback buffer: Length in the buffer in the PC for transferring captured audio to PC sound system. Increased buffer size will ensure a smooth audio output but will also increase the delay between the capture of the audio stream and its playback.

Folders

Please select the directories in the PC for saving the captured images and audio, the saved Presets

DSC

DSC Work folder: Folder for DSC Work files.

DSC test content directory: Folder where DSC source bitmap files, related configuration files and DSC conversion tools are stored.

Automatically create missing content: When selected, compliance test tool During execution of DSC Compliance Tests, the tool automatically creates the DSC compressed content used for testing the DUT.

Keep auto-created DSC content files: By default, the DSC compressed content is deleted after use. If selected, the content is not kept, not deleted.

Warning Keeping the automatically created DSC compressed content will shorten the time needed for running the DSC compliance tests.

Please note, that the space needed for storing the full library **can be very large** (appr. 200 GBytes). Please make sure that the content will be stored in a medium that has the required space available.

Misc. options

Apply color conversions to saved images: When saving captured frames, the Color Mode selected in *Video* tab will be applied also to saved images.

Bypass $4:2:x \rightarrow 4:4:4$ *conversions*: 4:2:2 and 4:2:0 images are previewed and stored as received, without pixel doubling.

HDCP protected monitor: Text appearing if the monitor where UCD Console is viewed is HDCP compliant and HDCP is enabled. This feature enables preview of captured HDCP encrypted content in *Video* tab.

TSI Integration

Selections for generating a workspace for TSI usage.

TSI Integration	
Enable TSI Integration	
Select when to append exported DUT test to 'RunTest' script	
Always append when exporting to a new file	\sim

Enable TSI Integration: When selected, TSI Integration tool (*Tools* > *TSI Integration*) is enabled. When exporting test parameters in Sink / Source DUT Testing, test code is also appended for execution with TSI.

Please refer to TSI Integration and Exporting Tests for TSI later in this document.

AUX Analyzer Options

Options for configuring the way data is presented in AUX Analyzer tab in Event Log.

Please find full description of the controls in chapter *Event Log / DP AUX Analyzer* later in this document.

TSI Integration

Tools > TSI Integration. Selections for generating a workspace for TSI usage.

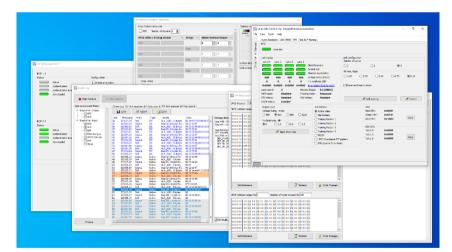
Use TSI x86 (32-bit)	
be used as 'sourcedevice' in scripts	
be used as 'sinkdevice' in scripts	
	be used as 'sourcedevice' in scripts

TSI Integration enables automatic creation of the necessary configuration files for executing tests exported from UCD Console's Sink DUT testing or Source DUT Testing.

Please refer to chapters *Source DUT Testing Tab* and *Sink DUT Testing Tab* later in this document for description about exporting tests.

Detaching Tabs

Most of the UCD Console tabs can be detached into a separate window for monitoring and controlling separate features simultaneously. To detach a tab **Right-click** on a tab and select **Detach Page**. To glue the tab back to the main window, click on the red **Close button** in the top right-hand corner of the window or press <Alt> + F4 on the keyboard.



6. DISPLAYPORT ALT MODE REFERENCE SINK

DisplayPort Alternate Mode Reference Sink function uses USB-C DP Rx interface.

DisplayPort Alternate Mode Reference Sink dialog is selected from the vertical tab (DP RX) on the left edge of UCD Console. Horizontal tabs on top of the GUI open controls for the various functions available for the interface. Some of the tabs are enabled by default, some only when an applicable license is included. DP RX contains the following functions.

- USB-C Monitoring dialog (USB-C)
- Video preview and saving (Video)
- Audio monitoring and saving (Audio)
- Status information and control of the upstream link (Link)
- EDID editor (EDID)
- DPCD editor (DPCD)
- HDCP status monitor and control (HDCP)
- SDP sent by the Source device (SDP)
- DSC capability control (DSC)
- FEC feature control and status (FEC)
- Source DUT Testing.

USB-C Monitoring

In *USB-C Monitoring* dialog operator can evaluate the status of the USB-C connection, the various roles adopted, and the configuration of the DP Alternate Mode. The user can set the initial roles for the UCD-424 TE and the optional capabilities for UCD-424 in the USB-C PD Contract. Controls allow user also to swap Power and Data roles. USB-C related panel can be selected from the **USB-C** tab on top of the GUI.

USB-C Monitoring dialog contains two horizontal tabs

- Roles and Modes
- Edit PDO Information
- Cable Info

Roles and Modes Sub-Tab

The **Roles and Modes** tab is divided into two parts: the left side is the **Status** panel while the right side provides the **Configuration** dialogs.

		esting \
Roles and Modes Edit PDO	Information Cable Info	
Status		Configuration
Power Role	PD Sink	CC Pull-up
Data Role	UFP	
Power Role Data Role	Cable info not available in UFP mode	O Default O 1.5A 💿 3.0A
VCONN	disabled	Initial Port Role
Current	Defined by power contract	In the Port Note
VCONN Current DP Alt Mode status	C: DPv1.4 4 lanes	DRP V
DP Alt Mode signalling DP Alt Mode config	DP v1.3	
DP Alt Mode config	Set UFP_U as UFP_D	DP Alt Mode (DFP)
Fixed supply PDO		Auto enter on connect 4 lanes (C,E)
DP Alt Mode signalling DP Alt Mode config Fixed supply PDO Dual Power Role capable	no	Manual 2 lanes (D)
USB Suspend supported	no	
Externally powered	no	O Disable Exit
USB Communication capable		
Dual Data Role capable	no	DP Alt Mode Capabilities (UFP_D)
Voltage	9.00V	DP Alt Mode 4 lanes (C)
Current	3.00A	DP Alt Mode 2 lanes (D)
Contract RDO		
Object position	2	DP Alt Mode 4 lanes (E)
Give back flag	false	Multi-function preferred
Capability mismatch	no	
USB Comm. capable	yes	Swap
No USB suspend	no	
Operating current, A	0.9	Data role Power role VCONN
Maximum current, A	0.9	Prevent DUT swap requests
1. Fixed	5.00V / 3.00A	
2. Fixed	9.00V / 3.00A	VCONN Power role Data role
2.11000	5.007 / 5.004	
Pull-up	Strongest, 3.0A	
Vbus voltage	9.40V	
Vbus current	1.07A	
CC1 voltage	0.00V	
CC2 voltage	1.74V 0.00V	
Vconn voltage SBU-1 voltage	0.00V 0.27V	
SBU-2 voltage	2.69V	Accessories
550-2 Voltage	2.050	Audio Accessory Debug Accessory
DUT Connected		Cable Orientation: Flipped Reconne

Status

The status panel lists the various roles and statuses of UCD-424 after the connection negotiation with the USB-C DUT.

The uppermost group indicates the general statuses like *Power Role* and *Data Role DP Alt Mode Configuration*.

Fixed Supply PDO (Power Data Objects) lists the PD status settings for the connection party acting as *Source Port* (in the shown case UCD-424).

Contract RDO (Request Data Objects) lists the PD status settings for the connection party acting as *Sink Port*.

The lowermost group lists the actual measured values of the Vbus, CC lines and Vconn.

Configuration

Initial Port Role	Port Role			
DRP	~			
DP Alt Mode (DFP)				
Auto enter on connect	4 lanes (C,E)			
◯ Manual	2 lanes (D)			
◯ Disable	Exit			
DP Alt Mode Capabilities (UFP_D)				
✓ DP Alt Mode 4 lanes (C)				
✓ DP Alt Mode 2 lanes (D)				
DP Alt Mode 4 lanes (E)				
Multi-function preferred				

Initial Port Role: Defines the role which UCD-424 presents itself in the start of PD communication (both power and data role).

DP Alt Mode (DFP)

Auto enter on connect: Start mode discovery after connection and enter DP Alternate mode if suitable configuration is found.

Manual:

4 lanes (C,E): Restart mode discovery and advertise support for modes C and D (4 DP lanes).

2 *lanes (D):* Restart mode discovery and advertise support for mode D (2 DP lanes + USB SS).

Exit: Exit DP Alternate mode.

DP Alt Mode Capabilities (UFP_D)

Supported Pin Assignments declared in DisplayPort Capabilities discover message.

DP Alt Mode 4 lane (C): All 4 lanes reserved for DP Alt Mode

DP Alt Mode 2 lane (D): 2 lanes reserved for DP Alt Mode 2 lanes for USB SS

DP Alt Mode 4 lane (E): All 4 lanes reserved for DP Alt Mode. Pin assignment E for supporting USB-C to DP cables and adapters.

Multi-function preferred: When entering DP Alternate Mode, select mode D.

Swap

S١

The Swap buttons allows the user to request a swap of either Data role, Power role or the CC line where VCONN is applied.

vap		

Data role	Power role	VCONN
Prevent DUT swa	p requests	
	Power role	Data role

VCONN: Send VCONN_Swap message to request an exchange of Vconn Source.

Power role: Send PR_Swap message to request an exchange of power roles.

Data role: Send *DR_Swap* message to request an exchange DFP and UFP operation between Port Partners while maintaining the direction of power flow over Vbus.

Prevent DUT Swap Requests

When selected the corresponding Swap messages from DUT are ignored.



Accessories

Accessories	
Audio Accessory	Debug Accessory

Audio Accessory: Enable simulation of Audio Accessory support

Debug Accessory: Enable simulation of Debug Accessory support

Enabling *Audio Accessory* and *Debug Accessory* extends USB Type-C Connection State Machine with *.Accessory states. (Please refer to USB Type-C specification for details).

Note: Please note that UCD-424 does not support any physical connections for the Accessory functions. The selections enable only behavioural simulation.

Bottom Panel

DUT Connected non E-marked cable Cable Orientation: Straight	Reconnect
--	-----------

The control lights indicate presence of the USB-C connection (Plugged, Not Plugged), the type of cable (Passive, Active/E-marked, Unigraf electrical test cable) and Cable Orientation (Straight, Flipped).

With the button you can *Reconnect* the USB-C connection.

Edit PDO Information Sub-Tab

The *Edit PDO Information* tab is divided into two sub-tabs: *PD Source objects* and *PD Sink objects*. Both panels allow user to set the PD Contract parameters of UCD-424 TE.

Apply: Write the selections to UCD-424 registers.

Refresh: Update the dialog by reading UCD-424 registers.

USB-C Video Audio Link EDID			Source DUT Testing	\			
Roles and Modes Edit PDO Inform	nation Cable Info						
PD Source objects PD Sink object	cts						
	5V	9V	_				
J	Mandatory $ \smallsetminus $	Fixed >	1				
Max Current, mA	3000 🚔	3000					
Voltage, mV	5000 🚖	9000					
Peak Current, %	125% ~	110%	_				
May Davies anW	12576	110 /0					
, have over, new							
Max Voltage, mV							
Min Voltage, mV							
USB Suspend Supported			Coad PDO's	Save PDO's	Refresh	Apply	
USB Suspend Supported			Coad PDO's	Save PDO's	Refresh	Apply	
			_		Refresh		
USB Suspend Supported			_	Save PDO's	Refresh	Apply	t
			_		Refresh		t
			_		Refresh		t
			_		Refresh		t
			_		Refresh		t
DUT Connected	re and Sink		_		Refresh	Reconnect	t
	ce and Sink		_		Refresh		t

Roles and Modes Edit PDO Inform			
PD Source objects PD Sink obje			
	5V	9V	
	Mandatory 🗸	Variable ~	
Max Current, mA	900 🚔	900	
Voltage, mV	5000 🚔		
Max Power, mW			
Max Voltage, mV			
		9000	
Min Voltage, mV		5000 🖨	
PD Contract Settings		RDO flags	
Automatically negotiate pow	wer contract	Give Back Flag	
Use Battery PDO		No USB Suspend	
Use Variable PDO			
PDO type priority			🔄 Load PDC
Prefer higher current	~		Save PD0
Minimum required power			
Automatically calculate			Refresh
Minimum power, mW	500		
			Apply
			 , 46.1

Note: Please note that changes will be written to the UCD-424 registers only by clicking Apply.

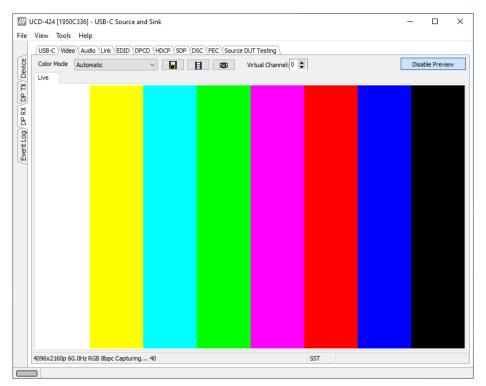
Cable Info Sub-Tab

The **Cable Info** tab displays the information received from the cable as a response to *Discover Identity* command sent to SOP'.

Roles and Modes Edit PDO information Cable Info 0000000 b4 04 00 1c 00		2f 08 00		
LISB Vendor ID	0484		XID Assigned by USB-IF	0x0000000
Modal operation supported	ves		All Ablighter by 660 I	0,0000000
Product Type	/	e Cable		
USB Communications Capable as USB Device	no			
USB Communications Capable as USB Host	no		bcdDevice	0x0000
			USB product ID	0xF681
USB SuperSpeed Signalling Support		USB 3.1 Gen1 and Gen2		
VBUS through cable		Yes		
VBUS Current Handling Capability		3A		
SSRX2 Directionality Support		Configurable		
SSRX1 Directionality Support		Configurable		
SSTX2 Directionality Support		Configurable		
SSTX1 Directionality Support		Configurable		
Cable Termination Type		VCONN required		
Cable Latency		<10ns (~1m)		
USB Type-C plug to USB Type-A/B/C/Captive		USB Type-C		
Firmware Version		0x0000		
Hardware Version		0x0000		
				Refresh

Click **Refresh** to read the data from an electrically marked cable.

Video Tab



Video tab is the Preview window for the captured DisplayPort stream.

Input video mode

7680x4320p 30.0Hz RGB 8bpc Capturing... 76

The measured input resolution, frame rate and color format are shown below the preview window. The indication of the number of frames captured to the PC indicates the pace of the image data transfer to the PC.

Disable / Enable Preview

Click here the button to start or stop capturing video frames.

The top ribbon of the tab has the following controls:

Color Mode for preview

YCbCr (ITU-709) -> RGB <

- No Conversion: The captured color components are interpreted as R, G and B respectively. No color conversion will be done.
- Automatic: The color mode is selected based on the information in the MSA. If there is no color information available, "No Conversion" is used.
- YCbCr (ITU-709) -> RGB: The captured data components are interpreted as Y, Cb, and Cr respectively. Color conversion to RGB is done based on ITU-709 standard.
- SMPTE 170M > RGB: The captured data components are interpreted as Y, U, and V respectively. Color conversion to RGB is done based on SMPTE 170M standard.

Note: Please note that the color mode selection applies to the preview window only. All internal functions use the raw image data as captured from the input channel.

Select Virtual Channel

When Multistreaming (MST) is enabled, the monitored stream can be selected here.

Save one frame



Capture and save one video frame as a bitmap file in the PC. The format and storage location can be selected in Tools > Options pull-down menu. The available bitmap formats are PPM, BMP and JPG.

The selections in Tools > Options menu define if the frame bitmap will be stored as captured from the display interface or if the color mode conversion selected for preview will be applied.

Sequence recording



Clicking the button opens a dialog for definition of number of frames recorded. Buffered mode can also be enabled in this dialog.



In buffered mode, all input frames are captured non-drop until the on-board frame buffer will be full. The dialog also informs the capacity of the buffer with the selected video mode.

In non-buffered mode, only one input frame is buffered at a time. Frames will be skipped if the transfer of the data to the PC is slower than the input data rate.

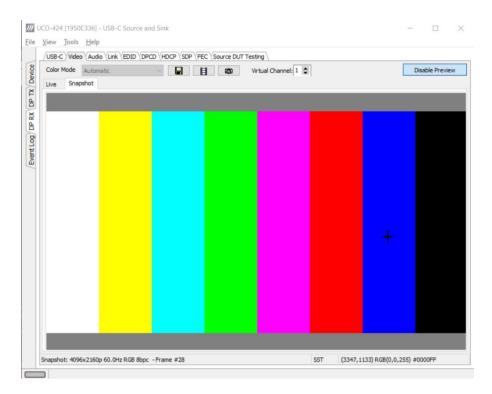
Note: Please note that buffered mode cannot be used when Audio preview is enabled.



Snap preview



When clicked, one frame of the incoming video is captured and shown in a new *Snapshot* tab. The captured bitmap can be saved with **Save one frame** function described above.



Color Information of the Captured Bitmap can be evaluated by placing the mouse cursor on top of the preview image. The lower right-hand side ribbon of the GUI lists

- Location of the cross cursor on the bitmap
- The intensity of the Red, Green and Blue components of the pixel on the cursor location
- The HTML HEX color code of the pixel on cursor location

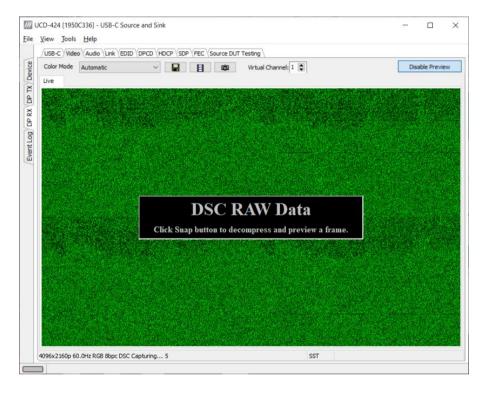
Zoom of the Preview Image can be altered by right clicking on top of the preview image and selecting between

- Fit Window
- Zoom 25%
- Zoom 50%
- Zoom 100%
- Zoom 200%
- Zoom 500%

While in the *Snap preview mode* clicking on the "Camera" icon will take additional snapshots

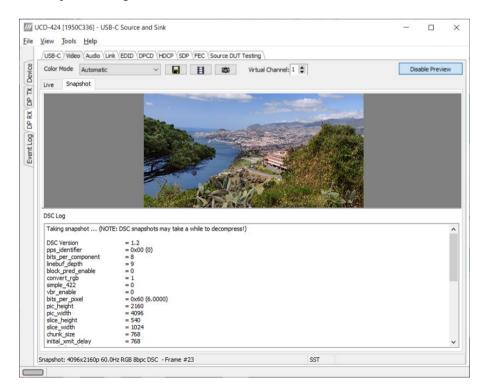
Preview DSC Decompressed Stream

In order to capture and preview DSC compressed video DSC must be enabled by selecting **Link Configuration > Other Capabilities > DSC** checkbox in *Link* tab.



Select Enable Preview to verify that DSC compressed stream is received.

Click **Snap a Frame** button to capture one frame and start the decompressor (offline in the PC). Once the decompression is ready, the frame is shown, and *DSC Log* lists the details of the compressed image.



Audio Tab

Audio tab has a preview of the audio signal format and the controls for audio playback and recording. Up to eight channels will be shown based on the received audio stream.

UCD-424 [1950C336] - USB-C So View Tools Help	urce and Sink					_	
USB-C Video Audio Link ED			OUT Testing				
Spectrum 60 dB \checkmark	 Virtual Cha 	nnel: 0 🌲 👔 r	Vo audio playback	~		Disable	e Preview
******	*****	*****	*****	*****	*****	*****	*****
	******	********	******	*****	******	~~~~	~~~~
	******	******	****	*****	******	~~~~	~~~~
	·····		·····			~~~~	~~~~
			·····			~~~~	~~~~
	*****	*****	****	·····		~~~~	~~~~
						ww	ww
8 channels; 44100 Hz; 16 bits				SST			22050

The audio signal format is shown in three ways

- The 'oscilloscope' panel displays the waveforms of the received audio channels.
- The frequency spectrum of the audio is shown in the lower panel. The range of the spectrum display is from 0 to 1/2 of the input sampling rate. The amplitude scale of the spectrum display can be selected between 'Linear' to 80 dB.
- The horizontal sound level indicator is in the bottom of the dialog.

The span of the preview window is defined with **Audio preview size** found in Tools > Options dialog. The value is given in ksamples (1024 samples). The relation between the preview window span in milliseconds (msec) and the value given in *Audio preview* size depends on the sampling frequency. Please do not exceed the *Audio buffer size* set in the same dialog.

Disable / Enable Preview

This button controls capturing the audio data.

Select Virtual Channel

When Multistreaming (MST) is enabled, the monitored stream can be selected here.



Playback device selection

The captured audio can be played back in the PC. The combo-box defines the audio device in the host PC through which the captured audio is played. By default, the *No audio playback* is chosen.

000 UCD-424 [1950C336] - USB-C Source and Sink	-		×
File View Tools Help			
/USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \			
Spectrum 60 dB Virtual Channel: 0 💭 Default audio playback device V	Disa	ble Previe	N
	******	*****	~~~
		~~~~	~~~

#### Note

Please note that the audio capabilities of the audio playback device of the PC are not automatically reflected in the audio capabilities description in UCD-424 EDID. Since UCD-424 is not performing any audio format conversion, it might occur that the source provides an audio format that the selected playback device is not supporting. In case a conflict occurs, please change manually the EDID content or disable audio playback to monitor the waveforms in UCD Console.

#### Refresh audio device list



Click here to re-read the list of audio devices after making changes to the host PC configuration.

#### **Audio Buffer Size**

The amount of buffering used in the data transfer between the UCD-424 unit and the PC in **Audio buffer size** in Tools > Options dialog. Increased buffer size will ensure a smooth audio output but will also increase the delay between the capture of the audio stream and its playback.

#### Start audio recording



The captured audio can be recorded in the PC using Waveform Audio File Format, WAV (*.wav) format. The pop-up dialog defines recording duration. The folder where the audio file will be saved can be selected in File > Options.

Recording			×
Recording duration, msec:	5000	✔ ОК	X Cancel

#### Input audio mode

2 channels; 48000 Hz; 16 bits

This field (in the bottom of the dialog) indicates detected audio mode in the input stream.

# Link Tab

Link tab contains four panels: Cable / HPD, Link Status, Link Configuration and Stream Status.

View Tools				DSC \FEC \Source	DUT Testing \			
Cab	le 🗖	HPD	🗸 Assert	S Deasse	rt 💋 Pulse HPD	500 🔹 Length, m	Short Pi	
Link Status Lane 0 La	ne 1 Lane 2	Lane 3	Clock Recove	erv	Link Configuration Max Lanes	02	٠4	
600 6	500 600	600	Symbol lock Channel equ Voltage swin		Max Bitrate, Gbps 1.62 DP Bitrate, Gbps	70 🔿 5.40	○ 6.75	
	3.5 3.5 0000 0x000 4			s (dB) <u>(Click to clear)</u> <b>8.1 (HBR3)</b>	None 2.	16 0 2.43	03.24 04.32	
MST mode: FEC status:	Disabled Disabled		g mode: I	Enhanced Disabled	☐ MST ☑ TPS3 ☑ TPS4 ☑ FEC ☐ DSC Scrambler reset			
HDCP status: Scrambling:	Disabled Enabled				FFFFh (DP) OFFFEh (eDP ASSR) O Custom 0x FFFF			
SSC Status:	Disabled				Enable fast LT	Force cable sta	Apply	
							🔮 Update Link Statu	
Stream Status Horizontal		Vertical		Misc		CRC	DSC CRC	
Total: Start: Active:	4400 216 4096	Total: Start: Active:	2250 82 2160	Frame Rate, Hz Color Depth: 8	: 0.000	Red:         0x3F3A           Green:         0x967D           Blue:         0xA7BF	Value 0: 0x0000 Value 1: 0x0000 Value 2: 0x0000	
Sync Width:	(+) 88	Sync Width:	(+) 10	Color Encoding: RGB unsp.	(legacy RGB mode)	Сору	Copy	

#### Cable / HPD

Indicator lights of the state of the cable. **Cable** indicates that the hardware has detected an upstream cable. **HPD** indicates that the HPD signal is Asserted (logical "high").

Clicking the **Deassert** button will cause HPD line to be set to logical "low" (de-asserted) and hence no HPD pulse can be generated. Click the **Assert** to re-activate the HPD line (set to logical "high").

To apply an HPD Pulse with programmable duration click **Pulse HPD**. The duration will be defined in the provided field.

For applying a short pulse click Short Pulse. Pulse duration is 1 ms.

#### Link Status

Link Status displays the status of the link training and the link parameters negotiated between UCD-424 Sink and the Upstream Source. The data is retrieved from the DPCD registers of the UCD-424 Sink. The status is updated automatically.

#### Link Configuration

Link Configuration allows the user to change the way the Sink capabilities are announced in the DPCD registers of the UCD-424 Sink. Maximum Lane Count, Maximum Bitrate and supported eDP Bitrate are set with their appropriate radio buttons.

To update the new status to the DPCD registers click **Apply**.

Note: Please note that UCD Console Link Tab currently supports for announcing one bitrate from the pre-selected rates to be used with eDP protocol. The user can apply alternative schemes by editing DPCD register content in the DPCD Tab.

<u>Other Capabilities</u> Enable or disable features like MST, FEC and DSC

Scrambler Reset

Selection of the value to which the Linear Feedback Shift Register (LFSR) is reset during scrambler reset.

In **Auto** mode UCD verifies that connected DP Sink supports eDP and Alternate Scrambler Seed, and then applies FFFEh. If not, FFFFh will be used.

When **Force cable status to plugged** is checked, sink functionality is active regardless of a failure of upstream device detection e.g., due to incorrect AUX Channel electrical termination.

Click Enable Fast LT to enable support for a link training without AUX transactions.

To apply a Hot-Plug Detect pulse automatically after updating the status, select **Generate HPD pulse on Apply**. HPD pulse duration will be defined in the *Pulse* HPD field.

#### **Stream Status**

Stream status is enabled with UCD Pro for DP Sink license.

Video Timing Details are retrieved from the Main-Stream Attributes (MSA) of the monitored stream. Frame rate is measured by UCD-424 Local Sink.

Note: Please note that the MSA information used for Video Timing Details is provided by the Upstream Source, it is not measured by the UCD-424 Local Sink.

#### CRC

The 16-bit **CRC** (checksum, cyclic redundancy check) values of the three color components calculated by the Sink hardware. To re-calculate, click **Update Link Status**.

The 16-bit **DSC CRC** values of the captured DSC compressed frame. "**Value 0**" is calculated from  $1^{st}$ ,  $4^{th}$ ,  $7^{th}$  ... byte, "**Value 1**" from  $2^{nd}$ ,  $5^{th}$ ,  $8^{th}$  ... byte and "**Value 2**" from  $3^{rd}$ ,  $6^{th}$ ,  $9^{th}$  ... byte.

### Multistreaming

When Multistreaming (MST) is enabled, and the source sends a multi-stream signal the details of the received virtual channels is shown in a table in *Stream Status* field.

		dio 🛛 Link		DPCD (HD	ICP (SDP	VDSC VFE	EC \Sourc	e DUT Testir	ng \							
Cable / H	IPD Cable		HP	D	🗸 Asse	rt	🚫 Deas	ssert	💋 Pul:	se HPD	500 ×	Length, ms	ec	💋 Shor	rt Pulse	
Link Stat		1 Lane	2 1	ane 3				Link Co Max La		tion						
cone o					lock Reco	overy		01			<b>2</b>		• 4			
					ymbol loc	k		Max Bi	trate, 0	Sbps						
						qualization		0 1.6	2	02.70	0	5.40	O 6.75	08.1	0	
800	800				-	ving (mVpp	)	eDP Bit	rate, G	bps						
3.5	3.5		-		re-empha			○ Nor	ne	0 2.16	0	2.43	03.24	04.3	2	
0x0000			)00 Ox			nt (Click to		Other	Capabil	ities						
Lane cou	Lane count: 4 Bit rate (Gbps): 8.1 (HBR3)					R3)	MMST MTPS3 MTPS4 MFEC DSC									
MCT more	de la	Enabled	•	Eromina	mode	Enhanc	hod	∠ MST			Scrambler reset					
MST mod		Enabled		Framing DSC stat		Enhanc					2					
MST mod FEC stat HDCP st	tus:	Enabled Disable Disable	d	Framing DSC stat		Enhanc Disable		Scramb	oler res	et	Eh (eDP ASS		ustom 0x FFF	F ¢		
FEC stat	tus: atus:	Disable	d d	-				Scramb	oler res Fh (DP)	et OFFF	Eh (eDP ASS	ir.) O CL	istom 0x FFF			
FEC stat HDCP st	tus: atus: ng:	Disable Disable	d d I	-				Scramb	oler res Fh (DP)	et OFFF	Eh (eDP ASS	ir.) O CL				
FEC stat HDCP st Scrambli	tus: atus: ng:	Disable Disable Enabled	d d I	-				Scramb	oler res Fh (DP) ble fas	et OFFF	Eh (eDP ASS	ir.) O CL	ustom 0x FFF			
FEC stat HDCP st Scrambli	tus: atus: ng:	Disable Disable Enabled	d d I	-				Scramb	oler res Fh (DP) ble fas	et OFFF	Eh (eDP ASS	ir.) O CL	ustom 0x FFF	d		
FEC stat HDCP st Scrambli SSC Stat	tus: atus: ng:	Disabler Disabler Enabled Disabler	d d l d	-			ed.	Scramb	oler res Fh (DP) ble fas	et OFFF	Eh (eDP ASS	ir.) O CL	ustom 0x FFF	d 🖌 Apply		
FEC stat HDCP st Scrambli SSC Stat	atus: ng: tus:	Disabler Disabler Enabled Disabler	d d l d	DSC sta		Disable	ed Frame ra	Scramb	oler res Fh (DP) ble fas	et OFFF	Eh (eDP ASS	ir.) O CL	ustom 0x FFF	d 🖌 Apply	tatus	
FEC stat HDCP st Scrambli SSC Stat	ed virtual	Disable Disable Enabled Disable	d d l d	DSC sta ream #0	tus:	Disable	ed Frame ra V-Sync	Scramb Scramb FFFI Ena Gen ate, Hz: 59.9	oler res Fh (DP) ble fas erate H 995 BPC	et CFFF t LT HPD pulse	Eh (eDP ASS	R) OCL	us to plugge	d ✓ Apply date Link St	tatus	
FEC stat HDCP st Scrambli SSC Stat	ed virtual	Disable Disable Enabled Disable disable	d d i d H-Sync (+) 88 (+) 44	DSC star ream #0 V-Total	tus: V-Start	Disable V-Active	Frame ra V-Sync (+) 10 (+) 5	Scramb FFFI Ena Ger ate, Hz: 59.5 CEF RGB unsp. (k RGB unsp. (k	erate H 995 BPC 8	HPD pulse	Eh (eDP ASS Force on Apply Stream ID	R) OCL e cable stat	Istom 0x FFF us to plugge	d Apply date Link St First slot	tatus Slot nu	
FEC stat HDCP st Scrambli SSC Stat Monitor H-Total 4400	ed virtual H-Start	Disabled Disabled Enabled Disabled Disabled H-Active 4096	d d l d H-Sync (+) 88	DSC star ream #0 V-Total 2250	V-Start 82	Disable V-Active 2160	Frame ra V-Sync (+) 10	Scramb FFFI Ena Gen Gen ate, Hz: 59.5 CEF RGB unsp. (k	erate H BPC 8 8 8	HPD pulse	Eh (eDP ASS Force on Apply Stream ID 1	R) OCL e cable stat	Alloc. PBN 2160	d Apply date Link St First slot	tatus Slot no 36	

Port#: Port number where the virtual channel is directed.

Stream ID: Stream identification number of the virtual channel

Req. PBN: Requested PBN (payload Bandwith Number) value for the virtual channel

Alloc. PBN: PBN value allocated for the virtual channel

*First slot*: Time slot where the first VC Payload for the virtual channel is stored *Slot num*: Number of VC Payload slots reserved for the virtual channel.

# EDID Tab

EDID Tab provides tools for accessing the EDID of the UCD-424 Sink presented to the Upstream Source Device. There are three basic functions:

- Load and save EDID data files in the host PC
- Edit the EDID contents
- Program and read the contents of the EDID memory of up to four virtual MST Ports

<i>///</i> เ	JCD-424 [1	950C3	336] - U	SB-C S	ource	and Si	nk								-	×
File	View To	ols	Help													
	/USB-C	/ideo	Audio	Link /						Sourc	DUT Test	ing				
Device	EDID Data	:												EDID Files		
Dev	000000	00	ff ff	ff f	fff	ff 00	54 c7	36 40	4c 3	4 32 30			^	EDID Files		
Ĩ	000010													Load		
B	000020													Save as		
X	000040	35	00 5f	59 2	1 00	00 la	56 5e	00 a0	a0 a	0 29 50				Save as		
B	000050															
Event Log	000070													HEX Editor		
eut	000080														_	
E L	000090 0000a0													Clear		
	0000b0	00	00 00	00 0	0 00	00 00	00 00	00 00	00 00	0 00 00				Append file		
	0000c0															
	0000e0													EDID Editor		
	0000f0	00	00 00	00 0	0 0 0	00 00	00 00	00 00	00 0	0 00 50				EDID Editor		
														Virtual Channel		
														3	1	
														Sink EDID	1	
														SILIK EDID		
														Read		
														Write		
													~	write		
													-			

#### **EDID Files**

Note

With **Load...** and **Save as...** a hex EDID file can be read and written from the PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

Four blocks (512 bytes) of EDID code is read. If the device is not supporting all four blocks, the non-supported area is replaced with zeroes.

Currently the EDID Editor does not support Display ID. Hex EDID files can however be modified with the HEX Editor or externally generated hex EDID files that have Display ID content can be load and programmed into the hardware.

#### **HEX Editor**

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. EDID contents can be edited by typing over the existing values. Altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

After editing the data can either be saved to an *.ecd file in the PC with **Save as...** or programmed it to the hardware EDID memory with **Write**.



#### **EDID Editor**

EDID Editor is launched in a separate pop-up window. Please see the description of the EDID editor in Chapter <u>EDID Editor</u> later in this document.

Collection 1     Blocks in collection     Block 0 [VESA EDID]	Details of ":/0/Version/18-Byte data blocks/I Current Value = Detailed Timing Descriptor	Descriptor 1"	
- Checksum	New Value:		
✓ Version —Extension flag	Detailed Timing Descriptor		~
<ul> <li>Vendor &amp; Product ID</li> <li>Basic Display Parameters and F</li> </ul>	🖌 Set 😨 Quick Conf	g	
> Display x,y Chromacity coordini	Details of ":/0/Version/18-Byte data blocks/I	Descriptor 1"	
Established timings I and II     Manufacturer's Timings	Key	Value	^
> Standard Timings	Pixel Clock	533250	
✓ 18-Byte data blocks	Horizontal addressable video	3840	
> Descriptor 1	Horizontal Blanking	160	
> Descriptor 2	Vertical addressable video	2160	
> Descriptor 3 > Descriptor 4	Vertical blanking	62	
✓ Block 1 [CEA 861]	Horizontal Front Porch	48	
Checksum	Horizontal pulse width	32	
<ul> <li>CEA Extensions Version</li> </ul>	Vertical Front Porch	3	
···· Sink Underscans IT video	Vertical pulse width	5	
····Basic audio ····YChCr (4:4:4)	Horizontal Video Size	607	
YCbCr (4:4:4)	Vertical Video Size	345	
< >	La successione and the second se		*

# **DPCD** Tab

	Number of bytes to read: 0	x 100		
000010 00 00 00 00				
$\begin{array}{ccccccc} 0&0&0&0&0&2&1&8&3c&28\\ 0&0&0&4&0&0&0&0&0&0\\ 0&0&0&5&0&0&0&0&0\\ 0&0&0&0&0&0&0&0&0\\ 0&0&0&0&0$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	00 00 00 00 00 00 93 81 84 00 00 00 00 00 0	VickSink Device Status SINK_COUNT [RO] 0x00200 := 0x41 SINK_COUNT = 1 CP_READY = 1	
Set Reference	٢	Refresh 🥳 Write Changes		
DPCD Address range: 0x 200	) Number of bytes to read: 0	x 100		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	01 03 11 11 00 00 00 00 00 00 00 80 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00 00		

DPCD tab is a tool for monitoring and editing the DPCD registers of the UCD-424 Sink.

The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

The combo box above the DPCD Decoder window allows selection of how the DPCD data is interpreted. It can be either as  $DP \ 1.4 \ DPCD$ , or as  $DP \ 1.4 \ DPCD$  with Detailed Capability Info selected or not (DETAILED_CAP_INFO_AVAIL = 1/0).

Click Refresh to re-read the data from the DPCD registers to the window in question.

Click **Write Changes** to write the portion of data shown in the window in question to the DPCD registers.

Click Set Reference to store currently shown data as a reference for comparison.

When the data is *Refreshed* from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with **red** color.

USB-C Video A	udio (Link (EDID		P \{FEC \{Source DUT Test	ing			
DPCD Decoder 1.	4 + DETAILED_CA	AP_INFO_AVAIL = 0	~			🔁 Load	🔛 Save
DPCD Address rang	e: 0x 0	Number of bytes t	to read: 0x 100				
000010 00 00 000020 00 00 000032 24 10 000040 00 00 000050 00 00 000050 00 00 000050 00 00 000080 00 00 000090 bf 00 0000b0 00 00 0000b0 00 00	0         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00 </td <td>$\begin{array}{cccccccccccccccccccccccccccccccccccc$</td> <td>00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00&lt;</td> <td>~</td> <td>LANE0_1 0x00202 LANE0 LANE0 LANE0 LANE1 LANE1</td> <td>Device Status _STATUS [RO] := 0X77 _CR_DONE = 1 _OHANNEL EQ_DONE = 1 _SYMBOL_LOCKED = 1 _CR_DONE = 1 _CHANNEL_EQ_DONE = 1 _SYMBOL_LOCKED = 1</td> <td></td>	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00         00<	~	LANE0_1 0x00202 LANE0 LANE0 LANE0 LANE1 LANE1	Device Status _STATUS [RO] := 0X77 _CR_DONE = 1 _OHANNEL EQ_DONE = 1 _SYMBOL_LOCKED = 1 _CR_DONE = 1 _CHANNEL_EQ_DONE = 1 _SYMBOL_LOCKED = 1	
Set Referen		1	🗊 Refresh	Write Changes	=		
DPCD Address rang		Number of bytes t		^	-		
000210 00 80 000220 00 00 000230 00 00 000240 53 61 000250 00 00	00 80 00 80 00 00 00 00 00 00 00 00 53 6f 53 6f 00 00 00 00 00	00       80       00       00       00         00       00       00       00       00       00         20       00       00       00       00       00         00       00       00       00       00       00	0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0         0       0       0       0       0       0       0       0				
				~			
Set Referen	-e		🕼 Refresh	😴 Write Changes			

### Saving and Loading DPCD Content

DPCD data in the selected address areas can be saved as a file in your PC. There are three alternative formats:

- Binary *DPCD Fata File* format (*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- Comma Separated Values (*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (*.HEX) in a human readable text format.
- Click **Save** to select the location and the format of the file.
- Click **Load** to load DPCD data saved in *DPCD Data File* (*.DPD) format to the editor.
- To program the data into the DPCD registers of UCD-424 Local Sink click Write Changes.

Note	<ul> <li>Writing DPCD data to the DPCD registers of the UCD-424 Local Sink will potentially affect the status and capabilities of UCD-424 as seen by the upstream source.</li> <li>User control like Link Training or mode changes will modify the content of the DPCD registers</li> <li>During a reboot of UCD-424 the DPCD registers will be returned to their default</li> </ul>
	values

# HDCP Tab

HDCP tab is the dialog for monitoring the HDCP (for *High-Bandwidth Digital Content Protection*) status and controlling the HDCP capabilities of the UCD-424 device.

m	UCD-424 [19500	[336] - USB-C Source and Sink		-	×
File	View Tools	Help			
	USB-C Video	Audio Link EDID DPCD HDCP	SDP (DSC (FEC Source DUT Testing)		
Event Log/ DP RX (DP TX ) Device	HDCP 1.3 Status	Active Authenticated	Configuration HDCP Capable Keys Production Facsimile - "Test" None		
Eve	HDCP 2.3 Status	Active Authenticated Dedared as HDCP capable Keys loaded	Configuration HDCP Capable Keys Production Facsimile - "Test" - R1 Facsimile - "Test" - R2 None		

#### Status

The status field indicates the HDCP status of the UCD-424 device.

Active: The link between UCD-424 and the upstream source has been encrypted.

*Authenticated*: The HDCP handshake between the UCD-424 and the sink unit has been completed successfully.

Declared as HDCP capable: The UCD-424 unit recognizes HDCP handshake messages.

Keys loaded: The HDCP keys are loaded to the UCD-424 unit.

#### Configuration

HDCP Capable: To disable HDCP uncheck the box.

#### Keys

Select between Production or Facsimile HDCP keys. To remove the keys, select None.

#### HDCP 1.3 vs. HDCP 2.3

UCD-424 devices support by default both HDCP 1.3 and HDCP 2.3 standard.

# SDP Tab

SDP Tab is enabled with UCD Pro for DP Sink license.

In SDP Tab shows the *Secondary-Data Packets* sent by the Source device. Click **Update** to re-read the data.

		24 [19 Too				B-C	Sou	rcea	and S	Sink																						_				×
_	/USE	B-C ∖Vi				Link	EDI		PCD	HD	CP)	SDP		sc \r	EC	Sou	ırce	DUT	Test	ting																
/Event Log/ DP RX (DP TX / Device )	SDF		HB 0 00 00 04 06 0A	1 01 02 04 06 0A	2 17 00 04 06 0A	3 48 07 04 06 0A	PB 0 00 00 E2 BA 21	1 03 36 69 0D B4	2 91 40 E7 40	3 00 98 6F E4 03	4 00 00 E2 BA 21	5 03 36 69 0D B4	6 91 40 E7 40 82	7 00 A8 6F E4 03	8 00 00 E2 BA 21	9 03 36 69 0D B4	10 91 40 E7 40 82	11 00 88 6F E4 03	12 00 00 E2 BA 21	13 03 36 69 0D B4	91 40 E7 40 82	00 88 6F E4 03	00 00 A8 9E 1B	80 36 AC 70 60	00 40 85 E8 7E	00 88 F9 45 AE	00 00 A8 9E 1B	80 36 AC 70 60	00 40 85 E8 7E	00 88 F9 45 AE	00 A8 9E 1B	80 36 AC 70 60	00 40 85 88 7E 00	00 88 F9 45 AE	000 A8 9E 1B	80 36 AC 70

SDP Tab displays in hexadecimal format the following received SDP packets:

- Audio_TimeStamp
- Audio_Stream
- Extension
- Audio_CopyManagement
- ISRC
- Video Stream Configuration (VSC)
- Camera Generic 0
- Camera Generic 1
- Camera Generic 2
- Camera Generic 3
- Camera Generic 4
- Camera Generic 5
- Camera Generic 6
- Camera Generic 7
- Vendor-Specific Infoframe packet
- AVI InfoFrame packet
- Source Product Descriptor InfoFrame packet
- Audio InfoFrame packet
- MPEG Source InfoFrame packet
- Dynamic Range and Mastering InfoFrame
- Picture Parameter Set (PPS)

# DSC Tab

DSC Tab is enabled with DSC Decoder license.

DSC tab contains control of the Display Stream Compression (DSC) feature, and definition of DSC support capabilities that UCD-424 defines in its DPCD register.

UCD-424 [1950C336] - USB-C Sou	urce and Sink			-		×
View Tools Help						
USB-C Video Audio Link ED		Source DUT Testing				
DSC Capable	DSC Enabled					
DSC Major Version:	1	DSC Minor Version:	2			
RC block size:	65536 bytes $\sim$	RC buffer size, in blocks:	4			
Bits per Pixel Increment:	1/16 bpp $\sim$	Block Prediction:	Supported v	1		
Throughput mode 0:	340MP/s $\checkmark$	Throughput mode 1:	340MP/s ~	1		
Line Buffer depth:	9 bits $\sim$	Maximum Slice Width:	2560			
Supported Color Depths	Supported Color formats	H-Slice Capabilities				
8 Bits per color channel	RGB	✓ 1 Slice / DSC Sink	10 Slices / DSC Sink			
✓ 10 Bits per color channel	VCbCr 4:4:4	2 Slices / DSC Sink	12 Slices / DSC Sink			
✓ 12 Bits per color channel	Simple YCbCr 4:2:2	4 Slices / DSC Sink	16 Slices / DSC Sink			
	Native YCbCr 4:2:2	6 Slices / DSC Sink	20 Slices / DSC Sink			
	YCbCr 4:2:0	8 Slices / DSC Sink	24 Slices / DSC Sink			
	属 Reset Def	aults 🕼 Refresh	V Apply			
				-		
				_		
	View Tools Help /USB-C \Video \Audio \Link \ED DSC Capable DSC Major Version: RC block size: Bits per Pixel Increment: Throughput mode 0: Line Buffer depth: Supported Color Depths Ø 8 Bits per color channel Ø 10 Bits per color channel	/USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC         DSC Capable       DSC Enabled         DSC Major Version:       1         RC block size:       65536 bytes         Bits per Pixel Increment:       1/16 bpp         Throughput mode 0:       340MP/s         Supported Color Depths       Supported Color formats         M B Bits per color channel       M CBB         M 10 Bits per color channel       YCbCr 4:4:4         M Simple YCbCr 4:2:2       Native YCbCr 4:2:2         M Keive YCbCr 4:2:2       YCbCr 4:2:2	View Tools Help           /USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \           DSC Capable         DSC Enabled           DSC Major Version:         1           RC block size:         65536 bytes           Bits per Pixel Increment:         1/16 bpp           Throughput mode 0:         340MP/s           Ythe Buffer depth:         9 bits           Supported Color Depths         Supported Color formats           Y CbCr 4:2:2         Y CbCr 4:2:2           Y Native YCbCr 4:2:2         Y CbCr 4:2:2           Y CbCr 4:2:0         9 Sits Since / DSC Sink	View Tools Help         /USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \         DSC Capable       DSC Enabled         DSC Major Version:       1         RC block size:       65536 bytes         RC block size:       65536 bytes         Bits per Pixel Increment:       1/16 bpp         Throughput mode 0:       340MP/s         Throughput mode 0:       340MP/s         Supported Color Depths       Supported Color formats         Maximum Slice Width:       2560         Supported Color Color channel       QCBC 4:4:4         I 10 Bits per color channel       QCBC 7:4:2:2         Q Native YCbCr 4:2:2       Q Slices / DSC Sink         I 2 Bits per color channel       QCBC YCbCr 4:2:2         Q Native YCbCr 4:2:2       Q Slices / DSC Sink         I 2 Bits per color channel       QCBC YCbCr 4:2:2         Q Native YCbCr 4:2:0       Q Slices / DSC Sink         I 2 Slices / DSC Sink       I 2 Slices / DSC Sink	View Tools Help         /USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \         DSC Capable       DSC Enabled         DSC Major Version:       1         RC block size:       65536 bytes         RC block size:       65536 bytes         Bits per Pixel Increment:       1/16 bpp         Throughput mode 0:       340MP/s         Juine Buffer depth:       9 bits         Supported Color Depths       Supported Color formats         YCbCr 4:4:4       YCbCr 4:4:4         YCbCr 4:2:2       YCbCr 4:2:2         Wative YCbCr 4:2:2       YCbCr 4:2:2         Wative YCbCr 4:2:0       2 Slices /DSC Sink         YCbCr 3:2:0       2 Slices /DSC Sink         YCbCr 4:2:0       8 Slices /DSC Sink	View Tools Help         /USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \         DSC Capable       DSC Enabled         DSC Major Version:       1         RC block size:       65536 bytes         RC block size:       1         DSC Major Version:       2         Incomponent:       11/16 bpp         Block Prediction:       Supported         Supported Color Depths       Supported Color formats         YCbCr 4:4:4       YCbCr 4:4:4         YCbCr 4:2:0       YCbCr 50S Clink          YCbCr 4:2:0       <

#### Enabling DSC

Enabling DSC feature is controlled by the connected source device. When connected, a source verifies corresponding registers in DPCD (0x00060) of UCD-424 sink to find out if DSC capability is declared.

*DSC Capable*: Control of UCD-424 DPCD register 0x00060 bit 0. Please click **Apply** to enable the change.

DSC Enabled: Connected source has enabled DSC

#### **DSC Support Capabilities**

The various controls in this tab change the content of UCD-424 sink DPCD register address range (0x00061 through 0x0006F) related to DSC. Please click **Apply** to enable the change.

#### Apply

Write changes to UCD-424 sink DPCD registers

#### Refresh

Re-read the content of UCD-424 sink DPCD and update the control status.

#### **Reset Defaults**

Reset the content of UCD-424 DSC related DPCD registers (0x00060 through 0x0006F) to the default values as defined in UCD-424 firmware.

# FEC Tab

FEC Tab is enabled as a basic feature.

FEC tab contains control of the FEC (Forward Error Correction) feature, Error Detection table and FEC Status Log.

USB-C Video Audio Link	C (CDID (DPC	UD (HDCP)	(ape (bac)			
FEC Capable	nerate HPD or	n change		FEC Enabled	FEC Status Log Disabled	
Error Counters (DPCD)					FEC Status: Decode Disable Detected	
	Lane #0	Lane #1	Lane #2	Lane #3	FEC Status: Decode Enable Detected Enabled, ready	
Uncorrected block errors	0	0	0	0		
Corrected block errors	0	0	0	0		
Bit errors	0	0	0	0		
Parity block errors	0	0	0	0		
Parity bit errors	0	0	0	0		
	Jpdate		Clear o	ounters		
	_a vdt		Clear o	ounters		

#### **Enabling FEC**

Enabling FEC feature is controlled by the source device. When connected, source verifies corresponding registers in sink DPCD to find out if sink is FEC capable. This register in UCD-424 sink can be controlled by **FEC Capable** checkbox.

Since source normally polls sink DPCD mainly after a new connection, selecting **Generate HPD on change** will force a new connection after the change of the FEC capability status.

- Click **Update** to read the FEC Error Counters
- Click **Clear** to clear the counters.

FEC Status Log lists FEC events.

## Source DUT Testing Tab

Please refer to Appendix E later in this document for description of the tests available.

UCD-424 [1950C336] - USB-C Source and Sink     View Tools Help		-		×
/USB-C \Video \Audio \Link \EDID \DPCD \HDCP \SDP \DSC \FEC \Source DUT Testing \				
Link-Layer Tests / HDCP 2.3 IA tests / HDCP 2.3 IB tests / CRC tests / Simple LT tests /				
< Test Name	Pass	Fail	Skip	Run
4 1A-01 Regular Procedure - With previously connected Receiver (With stored km)	1	0	0	1
2 🖌 🖌 1A-02 Regular Procedure - With newly connected Receiver (Without stored km)	1	0	0	1
↓ 1A-03 Regular Procedure - Receiver disconnect after AKE_Init	1	0	0	1
A-04 Regular Procedure - Receiver disconnect after km     IA-05 Regular Procedure - Receiver disconnect after locality check     No. 05 Regular Procedure - Receiver disconnect after locality check	1	0	0	1
1A-05 Regular Procedure - Receiver disconnect after locality check	0	0	0	0
<ul> <li>1A-06 Regular Procedure - Receiver disconnect after ks</li> </ul>	0	0	0	0
<ul> <li>1A-07 Regular Procedure - Receiver sends REAUTH_REQ after Ks</li> </ul>	0	0	0	0
<ul> <li>1A-08 Irregular Procedure - Verify Receiver Certificate</li> </ul>	0	0	0	0
- 1A-09 Irregular Procedure - SRM	0	0	0	0
<ul> <li>1A-10 Irregular Procedure - Invalid H'</li> </ul>	0	0	0	0
<ul> <li>1A-11 Irregular Procedure - Pairing Failure</li> </ul>	0	0	0	0
- 1A-12 Irregular Procedure - Locality Failure	0	0	0	0
☐ Configure [1	Import		] E	xport
Run Selected Stop on Failure Repeats: 1 🖕 Delay time, sec: 1 🛓 Save Report			Clear	All
Test Log:				
0003.151.353: [TE-Snk] STEP 1A-04-1 0003.753.083: [TE-Snk] WARNING. DUT sends unencrypted video 0003.753.214: [TE-Snk] DUT initiates authentication by transmitting AKE_Init 0003.753.804: Test PASSED: "IA-04 Regular Procedure - Receiver disconnect after km" *** Test complete PASSED ***				,
				`

Select the tests for execution by clicking the corresponding row.

Clicking **Configure...** opens a dialog for defining the test parameters for that set. Please refer to *Test Parameters* below for description.

Parameters from *Test descriptor files* can be loaded with **Import** and stored with **Export**. Please refer to chapter *Exporting Tests for TSI* later in this document.

Tests are started by clicking Run Selected. By clicking Abort the sequence is stopped.

Test flow can be controlled with **Repeats** of the test sequence, **Delay time** between individual tests or **Stop on Failure** that stops the whole sequence if one of the tests fail.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test, the matrix lists the number of occurrences of each result and the number of tries performed.

Click **Save Report** to generate a HTML report file for sharing the results with other parties for viewing without UCD Console.

By clicking Clear All the test log and the results matrix are cleared.

### **Test Parameters**

Each test set has its dedicated set of test parameters. Open a dialog for defining the parameters by clicking **Configure...**.

#### Parameters of Link Layer CTS

*Link Layer CTS* parameters includes DUT capabilities defined in *Source Device Capability Question List* in document *DisplayPort Link Layer Compliance Test Specification*. The capabilities are grouped into tabs based on the tested feature.

14	1000	Colorimet						
5000 1000 5000 5000	0	Sbpc V	ESA	8bpc ( 10bpc 8bpc (	CTA (ITU.601) : CTA (ITU.601) CTA (ITU.709)		8bpc CTA (ITU.601) 10bpc CTA (ITU.601) 8bpc CTA (ITU.709)	
Landa and L			1910 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 - 1917 -	10bpc	CTA (ITU. 709)	Ц	10bpc CTA (ITU. 709)	
		Select	Al					-
	~	Video Mor	tec					
1		Fall-cafe y	ideo mode:	164	0v400 @ 60Hz 6 B	PC		-
				100				~
		Maximum	supported thee mode.	30	HUXE TOO ID OUTE C	- DPC		-
		Most Pad	ed Timings					
rted		1 Lane	CTA 1440 x 576p @ 5	50Hz, 1	8 bpc			~
od wido		2 Lanes	CVT 1600 x 1200p @	60Hz.	RB1, 6 bpc			~
10 0000		4Lanes	CVT 2048 x 15360 @	60Hz.	RB1, 8 bor			~
					to a she			
		Time-stan	op generation					
			1 Lane		2 Lanes		4 Lanes	
		RBR	848x480@60 Hz	~ 1	280x720@60 Hz	×	1920x1080@60 Hz	~
		HBR	1280x720@60 Hz	~ 1	280x960@60 Hz	~	1920x1080@60 Hz	¥
		HBR2	1280x960@60 Hz	~ 1	920x1080@60 Hz	v	1920x 1080 @ 120 Hz	Y
		HBR.3	1920x1440@60Hz	~ 3	840x2160@30Hz	~	3840x2160@60Hz	4
Arthus Mideo								
	5000	1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 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1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 1000 • 10	5000     Sobe V       1000     Sobe V       5000     Sobe V       5000     Sobe V       10bpc     Bbpc V       10bpc     Bbpc V       10bpc     Sobe V </td <td>1000         Image: Constraint of the second se</td> <td>S000         RGB         N           1000         Image: Select ASA         Bbpc VESA         Bbpc VESA           5000         Image: Select ASA         Bbpc VESA         Bbpc VESA           100pc VESA         Bbpc VESA         Bbpc VESA         Bbpc VESA           4 Lanes         Image: Select AI         Image: Select AI         Image: Select AI           4 Lanes         Video Modes         Image: Select AI         Image: Select AI           4 Lanes         Video Modes         Image: Select AI         Image: Select AI           4 Lanes         Video Modes         Image: Select AI         Image: Select AI           4 Lanes         CVT 1600 x 12000 IP 60Hz, 4Lanes         Image: Select AI           4 Lanes         CVT 1600 x 12000 IP 60Hz, 1         Image: Select AI           4 Lanes         CVT 2048 x 15360 IP 60Hz, 1         Image: Select AI           4 Lanes         CVT 2048 x 15360 IP 60Hz, 1         Image: Select AI           4 Lanes         CVT 2048 x 15360 IP 60Hz, 1         Image: Select AI           4 Lanes         Image: Select AI         Image: Select AI           4 Lanes         Select AI         Image: Select AI           4 Lanes         Select AI         Image: Select AI           4 Lanes         Image: Select AI&lt;</td> <td>S000         RGB         YCbCr 4:2:2           1000         Stop: VESA         Bbp: CTA (TTU.601)           5000         Ibp: CTA (TTU.601)         Stop: VESA         Bbp: CTA (TTU.709)           5000         Ibp: CTA (TTU.709)         Stop: VESA         Bbp: CTA (TTU.709)           10bp: CTA         Ibp: CTA (TTU.709)         Stop: CTA         Bbp: CTA (TTU.709)           4 Lanes         Ibp: CTA         Ibp: CTA (TTU.709)         Stop: CTA           10bp: CTA         Ibp: CTA (TTU.709)         Stop: CTA         Stop: CTA           HBR3 (8.10 Gbps)         Video Modes         Stop: CTA         Stop: CTA           Herd         Maximum supported video mode:         3840x2160 @ 60Hz 6 B           Maximum supported video mode:         ILane         CVT 1600 x 1200p @ 60Hz, 8 B J, 6 Bpc           1Lane         CVT 1600 x 1200p @ 60Hz, 8 B J, 6 Bpc         Tme-stamp generation           1Lane         CVT 2048 x 1536p @ 60Hz, RB J, 8 Bpc         Tme-stamp generation           1Lane         1280x720@60 Hz         1280x20@60 Hz           HBR         1280x960@60 Hz         1920x1080@60 Hz           HBR         1280x960@60 Hz         1920x1080@60 Hz           HBR         1920x1440@60Hz         3840x2160@30Hz  </td> <td>S000         RGB         YCbCr 4:2:2           1000         Sbpc VESA         Bbpc CTA (TU.601)           5000         Sbpc VESA         10bpc CTA (TU.601)           5000         Sbpc VESA         Bbpc CTA (TU.709)           10bpc CTA         10bpc CTA (TU.709)         Sbpc VESA           10bpc VESA         Bbpc CTA (TU.709)         Sbpc CTA (TU.709)           10bpc CTA         10bpc CTA (TU.709)         Sbpc CTA (TU.709)           4 Lanes         Iobpc CTA         Select AI           HBR3 (8.10 Gbps)         Select AI         Select AI           Maximum supported video mode:         3840x2160 @ 60Hz 6 BPC           Maximum supported video mode:         3840x2160 @ 60Hz 6 BPC           ILane         CVT 1600 x 1200p @ 60Hz, RB1, 6 bpc           4 Lanes         CVT 2049 x 1536p @ 60Hz, RB1, 8 bpc           Tme-stamp generation         1 Lane         2 Lanes           HBR 1280x720@60 Hz         1 280x960@60 Hz         1 280x960@60 Hz           HBR 1280x920@60 Hz         1 920x1080@60 Hz         1 920x1080@60 Hz           HBR 1280x920@60 Hz         3840x2160@30Hz         1 920x1080@60 Hz</td> <td>S000         RGB         YCbCr 4:2:2         YCbCr 4:4:4           1000         Image: State of the st</td>	1000         Image: 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video mode:         ILane         CVT 1600 x 1200p @ 60Hz, 8 B J, 6 Bpc           1Lane         CVT 1600 x 1200p @ 60Hz, 8 B J, 6 Bpc         Tme-stamp generation           1Lane         CVT 2048 x 1536p @ 60Hz, RB J, 8 Bpc         Tme-stamp generation           1Lane         1280x720@60 Hz         1280x20@60 Hz           HBR         1280x960@60 Hz         1920x1080@60 Hz           HBR         1280x960@60 Hz         1920x1080@60 Hz           HBR         1920x1440@60Hz         3840x2160@30Hz	S000         RGB         YCbCr 4:2:2           1000         Sbpc VESA         Bbpc CTA (TU.601)           5000         Sbpc VESA         10bpc CTA (TU.601)           5000         Sbpc VESA         Bbpc CTA (TU.709)           10bpc CTA         10bpc CTA (TU.709)         Sbpc VESA           10bpc VESA         Bbpc CTA (TU.709)         Sbpc CTA (TU.709)           10bpc CTA         10bpc CTA (TU.709)         Sbpc CTA (TU.709)           4 Lanes         Iobpc CTA         Select AI           HBR3 (8.10 Gbps)         Select AI         Select AI           Maximum supported video mode:         3840x2160 @ 60Hz 6 BPC           Maximum supported video mode:         3840x2160 @ 60Hz 6 BPC           ILane         CVT 1600 x 1200p @ 60Hz, RB1, 6 bpc           4 Lanes         CVT 2049 x 1536p @ 60Hz, RB1, 8 bpc           Tme-stamp generation         1 Lane         2 Lanes           HBR 1280x720@60 Hz         1 280x960@60 Hz         1 280x960@60 Hz           HBR 1280x920@60 Hz         1 920x1080@60 Hz         1 920x1080@60 Hz           HBR 1280x920@60 Hz         3840x2160@30Hz         1 920x1080@60 Hz	S000         RGB         YCbCr 4:2:2         YCbCr 4:4:4           1000         Image: State of the st

#### Parameters of HDCP CTS

DP HDCP CTS 1A test parameters		_	- 🗆	×
Test Parameters				
Test timeout, milliseconds	200000			
Revoke ID	71.6A.15.46.BF			
Source_EncDisableBootstrapping	1			
Presets	🗸 ок		🗶 Cano	el

#### Parameters of CRC Test Set

CRC Video test parameters dialog contains fields for defining the test duration, number of frames captured, errors allowed and expected video format.

CRC Video test parameters					×
Base parameters		Refe	rence CRC's		
Test timeout (milliseconds):	10000		F3A, 0x967D		^
Run until timeout			F3A, 0x967D F3A, 0x967D		
Test length (# frames):	2000	×			
Errors allowed (# frames):	20	* *			
Repeat "Continuous motion picture te	st" until timeout				
Test iterations (# of repeats):	1	*			
Expected Video Signal					
Width (# pixels):	4096	<ul> <li>▲</li> <li>▼</li> </ul>			
Height (# pixels):	2160	•			
Reference BPP:	24 BPP	$\sim$			
Frame rate checking					
Enable frame rate check					$\sim$
Expected frame rate (mHz):	60000	CRC C	Capture length (	# frames)	
Frame rate tolerance (±mHz):	100	× 3	<ul> <li>T</li> </ul>	Capture now	
Presets		<b>~</b>	ОК	🗶 Cance	I

Click **Capture now** to record *Reference CRCs*. Please define the number of frames used as reference – either one or the number of frames in the predefined test sequence.

#### Parameters of DP RX Simple LT Tests

The parameters for DP RX Simple LT test set is a subset of DUT capabilities.

DP RX Simple LT test parameters			-		×
Test Parameters					
Test timeout, milliseconds	5000				
Max lanes count supported by DUT	4				
Max lane rate supported by DUT in 0.27Gbps	20				
Reserved for DUT Capabilities flags	0				
Reserved for DUT Test automation capabilities flags	0				
Long HPD pulse duration, milliseconds	1000				
Link training start timeout, milliseconds	5000				
Delay between test cycles, miliseconds	3000				
Presets		🗸 ок	;	Cancel	

#### Presets

In all parameter dialogs the selected parameters can be saved as Presets. Please click **Presets...** to save or recall a configuration.

### Exporting Tests for TSI

Unigraf UCD Console includes a feature rich Software Development Kit (SDK) for use in automated testing. The SDK is called Test Software Interface (TSI). TSI allows for an easy integration of Production and R&D testing routines into an automated test system environment. Please refer to TSI documentation found in additional Unigraf manuals for details.

The tests included in UCD Console's Source DUT Testing tab and Sink DUT Testing tab can be executed in TSI environment. A straightforward way is to use UCD Console's *Tools* > *TSI Integration* dialog to create the necessary files for TSI environment and use *Export* function in *DUT Testing* tabs to include the intended tests.

	Configure	Ľ	Imp	ort		Expor	t
<ul> <li>5.2.1.12 Downstream Stop on Timeout</li> </ul>			0	0	0	0	
<ul> <li>5.2.1.11 Downstream Stop on MOT Reset</li> </ul>			0	0	0	0	
5.2.1.10 Interleaved EDID and DPCD Receiver Capability Read			0	0	0	0	
5.2.1.9 Glitch Rejection			1	0	0	1	_

*Export:* Save parameters of the selected test to a file. If TSI Integration is enabled in Tools > Options, also the test is appended into 'Run Test' file in TSI workspace folder.

*Import:* Recall parameters from configuration file. If TSI Integration is enabled in Tools > Options, parameters are imported from a file in TSI workspace folder

# 7. DISPLAYPORT ALT MODE REFERENCE SOURCE

DP Reference Source function is using one output channel, DisplayPort Source (DP TX). The corresponding vertical tab can be seen on the left edge of the GUI.

The horizontal tabs on the top of the GUI enable the various functions available for the output channel. Some of the tabs are enabled by default, some only when an applicable license is included. DPTX features the following functions.

- USB-C Monitoring
- Video pattern generator (Pattern Generator)
- Audio generator (Audio Generator)
- Status information and control of the downstream link (Link)
- EDID editor (EDID)
- DPCD monitor (DPCD)
- HDCP status monitor and control (HDCP)
- FEC feature control and status (FEC)
- Sink DUT Testing Tab.

# **USB-C** Monitoring

In *USB-C Monitoring* dialog operator can evaluate the status of the USB-C connection, the various roles adopted, and the configuration of the DP Alternate Mode. The user can set the initial roles for the UCD-424 TE and the optional capabilities for UCD-424 in the USB-C PD Contract. Controls allow user also to swap Power and Data roles. USB-C related panel can be selected from the **USB-C** tab on top of the GUI.

USB-C Monitoring dialog contains two horizontal tabs

- Roles and Modes
- Cable Info



### Roles and Modes Sub-Tab

The **Roles and Modes** tab is divided into two parts: the left side is the **Status** panel while the right side provides the **Configuration** dialogs.

Roles and Modes Edit PDO Inform	nation Cable Info	
Status		Configuration
Power Role Data Role	PD Source DFP	CC Pull-up O Default 1.5A @ 3.0A
VCONN Current DP Alt Mode status	enabled Defined by power contract C: DPv1.4 4 lanes	Initial Port Role
DP Alt Mode signalling DP Alt Mode config	DP v1.3 Set UFP U as UFP D	DRP ~
Fixed supply PDO		DP Alt Mode (DFP) Auto enter on connect 4 lanes (C,E)
Dual Power Role capable USB Suspend supported	no no	Auto enter on connect     4 lanes (C,E)     Manual     2 lanes (D)
Externally powered USB Communication capable	no no	O Disable Exit
Dual Data Role capable Voltage	no 9.00V	DP Alt Mode Capabilities (DFP_D)
Current	3.00A	DP Alt Mode 4 lanes (C)
Contract RDO Object position	2 false	DP Alt Mode 2 lanes (D)
Give back flag Capability mismatch USB Comm. capable	no	
No USB suspend Operating current, A	yes no 0.9	Swap
Maximum current, A	0.9	Data role Power role VCONN
1. Fixed 2. Fixed	0.00V / 0.00A 0.00V / 0.00A	Prevent DUT swap requests VCONN Power role Data role
Pull-up	Strongest, 3.0A	
Vbus voltage Vbus current	9.48V 1.07A	
CC1 voltage CC2 voltage Vconn voltage	5.50V 1.74V 5.50V	
Vconn voltage Vconn current SBU-1 voltage	0.00A 2.69V	
SBU-2 voltage	0.27V	Accessories Audio Accessory Debug Accessory

#### Status

The status panel lists the various roles and statuses of UCD-424 after the connection negotiation with the USB-C DUT.

The uppermost group indicates the general statuses like *Power Role* and *Data Role DP Alt Mode Configuration*.

**Fixed Supply PDO** (Power Data Objects) lists the PD status settings for the connection party acting as *Source Port* (in the shown case UCD-424).

**Contract RDO** (Request Data Objects) lists the PD status settings for the connection party acting as *Sink Port*.

The lowermost group lists the actual measured values of the Vbus, CC lines and Vconn.

#### Configuration

*Initial Port Role:* Defines the role which UCD-340 presents itself in the start of PD communication (both power and data role).

#### **DP Alt Mode (UFP)**

DP Alt Mode (DFP) Auto enter on connect	4 lanes (C,E)
	2 lanes (D)
◯ Disable	Exit
DP Alt Mode Capabilities (DFP_D) DP Alt Mode 4 lanes (C) DP Alt Mode 2 lanes (D) DP Alt Mode 4 lanes (E)	

Auto enter on connect: Start mode discovery after connection and enter DP Alternate mode if suitable configuration is found.

#### Manual:

*4 lanes (C,E):* Restart mode discovery and advertise support for modes C and D (4 DP lanes).

2 *lanes (D):* Restart mode discovery and advertise support for mode D (2 DP lanes + USB SS).

Exit: Exit DP Alternate mode.

#### DP Alt Mode Capabilities (DFP_D)

Supported Pin Assignments declared in DisplayPort Capabilities discover message.

DP Alt Mode 4 lane (C): All 4 lanes reserved for DP Alt Mode

DP Alt Mode 2 lane (D): 2 lanes reserved for DP Alt Mode 2 lanes for USB SS

*DP Alt Mode 4 lane (E):* All 4 lanes reserved for DP Alt Mode. Pin assignment E for supporting USB-C to DP cables and adapters.

#### Swap

The Swap buttons allows the user to request a swap of either Data role, Power role or the CC line where VCONN is applied.

Swap		
Data role	Power role	VCONN
Prevent DUT sw	ap requests	
	Power role	Data role

*Data role:* Send *DR_Swap* message to request an exchange DFP and UFP operation between Port Partners while maintaining the direction of power flow over Vbus.

Power role: Send PR_Swap message to request an exchange of power roles.

VCONN: Send VCONN_Swap message to request an exchange of Vconn Source.

#### **Prevent DUT Swap requests**

When selected the corresponding Swap messages from DUT are ignored.

#### **Bottom Panel**

DUT Connected	non E-marked cable	Cable Orientation: Straight	Reconnect	

The control lights indicate presence of the USB-C connection (Plugged, Not Plugged), the type of cable (Passive, Active/E-marked, Unigraf electrical test cable) and Cable Orientation (Straight, Flipped).

With the button you can Reconnect the USB-C connection.

### Edit PDO Information Sub-Tab

The *Edit PDO Information* tab is divided into two sub-tabs: *PD Source objects* and *PD Sink objects*. Both panels allow user to set the PD Contract parameters of UCD-424 TE.

0-424 [1950C336] - USB-C Source a	and Sink					_		>
ew <u>T</u> ools <u>H</u> elp								
JSB-C \Pattern Generator \Audio Ge	enerator Link E			Testing				
Roles and Modes Edit PDO informatio			``````````````````````````````````					
PD Source objects PD Sink objects								
	5V	9V						
	Mandatory $\sim$	Fixed ~	1					
Max Current, mA	3000 🚖	3000						
Voltage, mV	5000 🚔	9000						
Peak Current, %	125% ~	110% 、						
	12570 -	11070						
Max Power, mW								
Max Voltage, mV								
Min Voltage, mV								
USB Suspend Supported			🔄 Load PDO's	Save PDO's	Refresh		Apply	
DUT Connected non E-ma	arked cable		Cable O	rientation: Straight			Reconnec	
								τ
)-424 [1950C336] - USB-C Source a	and Sink							t
ew <u>T</u> ools <u>H</u> elp				Testing				
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ew Iools Help USB-C \Pattern Generator \Audio Ge toles and Modes Edit PDO Informati PD Source objects PD Sink objects Max Current, mA Voltage, mV Max Voltage, mV Max Voltage, mV PD Contract Settings Automatically negotiate power Use Battery PDO PDO type priority Prefer higher current	enerator \Link \E ion Cable Info 5V Mandatory \ 900 \$ 5000 \$ contract	9V Fixed 1000	DCP \FEC \Sink DUT	Testing				5
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ew Jools Help JSB-C \Pattern Generator \Audio Ge koles and Modes Edit PDO Informati PD Source objects PD Sink objects Max Current, mA Voltage, mV Max Voltage, mV Max Voltage, mV PD Contract Settings Automatically negotiate power Use Battery PDO PDO type priority Prefer higher current Minimum required power Automatically calculate	enerator \Link \E ion Cable Info 5V Mandatory \ 900 \$ 5000 \$ contract	9V Fixed 1000	DCP \FEC \Sink DUT	Testing \		R	.oad PDO's Save PDO's effresh	

### Cable Info Sub-Tab

The **Cable Info** tab displays the information received from the cable as a response to *Discover Identity* command sent to SOP'.

	USB-C \Pattern Generator \Audio Generator \Link \E Roles and Modes Edit PDO information Cable Info 000000 b4 04 00 1c 00 00 00 00 00 00			esting \			
5 - 5 -	LISB Vendor ID	0484		XID Assigned by USB-IF	0x0000000		
5	Modal operation supported	yes		AD Assigned by 030-1	0x0000000		
5	Product Type		ve Cable				
	USB Communications Capable as USB Device	no					
	USB Communications Capable as USB Host	no		bcdDevice	0x0000		
1				USB product ID	0xF681		
~	USB SuperSpeed Signalling Support		USB 3.1 Gen1 and Gen2				
	VBUS through cable		Yes				
	VBUS Current Handling Capability		3A				
	SSRX2 Directionality Support		Configurable				
	SSRX1 Directionality Support		Configurable				
	SSTX2 Directionality Support		Configurable				
	SSTX1 Directionality Support		Configurable				
	Cable Termination Type		VCONN required				
	Cable Latency		<10ns (~1m)				
	USB Type-C plug to USB Type-A/B/C/Captive		USB Type-C				
	Firmware Version		0x0000				
	Hardware Version		0x0000				
					Refres	sh	

Click **Refresh** to read the data from an electrically marked cable.

Note Please note that only the port partner that is DFP mode communicates with the cable plug. Therefore, Cable Info is available only in DFP mode.

## Pattern Generator Tab

ISB-C / Pattern Ge Iideo Pattern Gene		rator \Link \ED	ILD Y DPCD YHDCP	FEC Sink DUT Testin	g \Custom image
		_			
MST Numb	er of streams 1	Force	EDID preferred tir	ning after LT	
CTA 4096x2160 @	60Hz (VIC 102)	✓ 8 bpc	✓ Color B	lars v	No.
RGB		~	1	÷ 1 ÷	
		_			
		✓ 8 bpc	$\sim$		
RGB			1	* 1 *	
		✓ 8 bpc	$\sim$		-
			1	1 A	Default.bmp
RGB		~	1	* 1 *	Click on image to load
		8 bpc			
RGB	$\sim$	$\sim$	1	1 A	
Timing values					
Custom		0			
	H-Total	4400			
	H-Start	216			Adaptive-Sync
	H-Active	4096			Auto-enable if supported by sink
	H-Sync Width	88			Disabled $\checkmark$
	V-Total	2250			
	V-Start	82			
	V-Active	2160			
	V-Sync Width	10			
	Frame Rate				
V-5	ync Negative polarity				DSC Status and Configuration
Mana	ge Timings				Enable DSC
					Pattern Generator Settings

Note

The video modes that can be used in MST streams are limited by the overall capability of the DisplayPort link and the capability of the connected DisplayPort Sink or Branch device.

#### **Predefined Timings**

UCD-424 includes a set of common predefined video timings. Please find a list of the timings with their major details in <u>Appendix C</u> of this document.

#### Force EDID Preferred Timing After LT

After Link Training (= plug-in) UCD applies the timing indicated as the Preferred Timing in VESA block of Sink device EDID.

The feature is disabled when MST mode is used.

#### **Color Mode**

RGB color mode with full range quantization levels will be used with all patterns except with *Color Square Pattern*. This pattern allows the user to select RGB, YCbCr 4:4:4, YCbCr 4:2:2 and YCbCr 4:2:0 color modes. When YCbCr is selected, the Colorimetry dropdown box is enabled and allows selection between ITU-709 and ITU-601. Please find a description of the available test patterns in <u>Appendix D</u> of this document.

#### **Color Depth**

You can set the color depth used. The available color depths are: 6, 8, 10, 12 and 16 bpc. Color depth 6 bpc is only available with RGB.

#### **Predefined Video Patterns**

UCD-424 has a set of predefined patterns and a possibility to user defined custom pattern. You can select the pattern in the provided combo box. By selecting **Disabled** you can have the links activated but no video data transferred.

Please find a description of the available test patterns in Appendix D of this document.

When MST mode is selected, full selection of test patterns is available only in stream 0

#### **Custom Image Patterns**

BMP, PNG, JPG and TIFF files can be loaded from the PC to be used as custom images. The bitmaps will be aligned to the top left hand side corner, displayed at the original resolution, no scaling, cropped to the active area.

#### **MST Operation**

Multi-streaming can be enabled from MST check box and selecting the number of streams.

Note	Please note that MST and DSC features and cannot be used simultaneously
------	-------------------------------------------------------------------------

#### Adaptive Sync Control

User controls in the four Adaptive Sync modes are the following.

- Adaptive Total, constant refresh rate: Added blank lines.
- Adaptive Total, Square pattern: Added blank lines, min; Added blank lines, max; Period, frames.
- Adaptive Vtotal, Zigzag pattern: : Added blank lines, min; Added blank lines, max; Increase, lines; Decrease, lines.
- Fixed Average VTotal: Target refresh rate, Hz; Increase, lines; Decrease, lines.

Auto enabled if supported by Sink enables the feature based on connected Sink status.

#### **Pattern Generator Settings**

In order to avoid sourcing invalid video mode combinations new settings are being validated when the user is clicking **Apply**. Automatic validation will be applied when **Auto-apply when valid** is checked. The situation that parameters have been changed but not applied is indicated by **bold values** of the parameter. If new settings cannot be supported by e.g. the selected link configuration, an error dialog will be shown.

USB-C Pat	ttern Generator Audio Ge	nerator Link E		CD HDCP FEC Sink DUT Testing	0
Video Patte	rn Generator				Custom image
MST	Number of streams 1	•		^	
Other 512	20 x 2880 @ 60.0Hz	✓ 10 bpc	- ×	Chessboa Error	X
RGB		$\sim$		1	
		∨ 8 bpc	$\sim$		etup failed due to: xel clock exceeds hardware capabilities
RGB		$\sim$		1	xer clock exceeds hardware capabilities
		✓ 8 bpc	$\sim$		
RGB				1	ок

Note Please note that the changes in Pattern Generator tab will not be applied unless the user validates them by clicking **Apply** or when **Auto-apply when valid** is checked.

#### **Custom Timing**

Custom Timing feature is enabled with UCD Pro for DP Source license.

Custom		0	1	2	3	
	H-Total	2200	2200	2200	2200	
	H-Start	192	192	192	192	
	H-Active	1920	1920	1920	1920	
	H-Sync Width	44	44	44	44	
	V-Total	1125	1125	1125	1125	
	V-Start	41	41	41	41	
	V-Active	1080	1080	1080	1080	DSC Status and Configuration
	V-Sync Width	5	5	5	5	-
	Frame Rate	60.000	60.000	60.000	60.000	Enable DSC
H-S	ync Negative polarity					Send PPS
V-S	ync Negative polarity					Pattern Generator Settings
Mana	ge Timings	1				 Apply Auto-apply when vali

The timing parameters can be modified by selecting the **Custom** check-box and editing the fields of the matrix. Enable the new parameters by clicking **Apply** button.

#### **Manage Timings**

Custom timings can also be created and edited with pop-up *Timing Editor*. Launch the editor by clicking **Manage Timings**.

/// Timing Edit	or							-		×
Current timings:										
Show/Type	Name		Timing v	/alues						^
<ul> <li>Fixed</li> </ul>	VESA 5120 x 2160 @ 60 VESA 5120 x 2160 @ 60 CTA 5120 x 2160 @ 60 VESA 5120 x 2160 @ 610 VESA 5120 x 2160 @ 12 CTA 5120 x 2160 @ 120 CTH 5120 x 2880 @ 60 VESA 7680 x 4320 @ 30 CTA 7680 x 4320 @ 30. VESA 7680 x 4320 @ 60	.0Hz [R DHz 0.0Hz [ 0.0Hz [ .0Hz .0Hz .0Hz [R .0Hz [R .0Hz [R DHz	Active ( Active ( Active ( Active ( Active ( Active ( Active ( Active (	5120 x 2160), Total (5120 x 2880), Total (580 x 4320), Total (7680 x 4320), Total (7680 x 4320), Total	(520 (550 (528 (520 (550 (550 (528 (784 (776 (900	0, 2222), Sync (32, 10) 0, 2222), Sync (32, 6) 0, 2250), Sync (88, 10) 0, 2287), Sync (32, 10) 0, 2287), Sync (32, 8) 0, 2250), Sync (32, 8) 0, 2250), Sync (32, 5) 0, 4381), Sync (32, 5) 0, 4381), Sync (32, 8) 0, 4400), Sync (176, 20) 0, 4443), Sync (32, 5)				~
Ac S Sync wi	Horizontal timing otal 5500 tive 5120 tart 216	Vertical tim 2250 2160 82 10 Negativ		Frame rate (Hz)     Pixel Clock (MH:	z)	120 1485 Can't modify fixed timing. CTA 5120 x 2160 @ 120.0F			Clear odate timi Id new tim	ing
							🗶 Cancel		🗸 ок	

In order to create a new custom timing based on one of the standard fixed, timings select the fixed timing and change its name and click **Add new timing** to store.

In order to modify an existing custom timing, select it, modify and click Update timing.

The dialog will make a sanity check for the values entered and will warn the user for any combinations that cannot be used.

#### **Customize Timings List**

The timings are shown on the pull-down menu by un-checking the **Show** box. The timings will remain in the list and can be brought back to the pull-down menu, when needed.

### Sourcing DSC Compressed Patterns

DSC compressed pattern files can be created with a separate tool called *DCS Compressor*. It can be launched from Tools > DSC Compressor.

SC Compressor	r					>
File to compress	;					
Source File:	C:\Te	mp\Your-image.png				
	4096	x 2160, 32bpp				
Sink DSC capabi	lity regis	ters (DPCD range 0x60 -	> 0x6f,	hex)		
					U	odate
Compression op	tions					
Color space to us	se:	Output resolutions:				
RGB	$\sim$	1920 x 1440	^	Compression Ratio:	8bpc -> 6bpp (4.0 to 1)	~
		2048 x 1536				
Color depth to us	se:	2560 x 1440		Horizontal Slices:	1 Slice	~
Color depth to us 8 bpc	se: ~	2560 x 1080		Horizontal Slices:	1 Slice	
				Horizontal Slices: Vertical Slices:	1 Slice	~
8 bpc Resize mode:		2560 x 1080 2560 x 1600 2880 x 1440 4096 x 2160	4			
8 bpc Resize mode: Tile / Crop	<b>~</b>	2560 x 1080 2560 x 1600 2880 x 1440	ł			
8 bpc Resize mode:	<b>~</b>	2560 x 1080 2560 x 1600 2880 x 1440 4096 x 2160 3840 x 2160		Vertical Slices:		

Select the source bitmap file in **Source File** field. Define the **Output Resolution**, the color depth, compression ratio and number of horizontal and vertical slices in the frame.

#### Click Start Compressor(s).

A DSC compressed file named e.g. *Your_Picture_4096_2160_8.dsc* will be created in the same folder are your source file *Your_Picture*. The selected resolution and bit depth will be added to the file name.

Video Pattern Gen	erator ber of streams 1			DCP (FEC (Sink DU	Custom image
CTA 4096 x 2160	@ 60.0Hz	✓ 8 bpc	<ul> <li>✓ DSC</li> </ul>	C Image	×
RGB		~	1	1	÷
		✓ 8 bpc	~		$\checkmark$
RGB			1	- 1	•
		✓ 8 bpc	$\sim$		×
RGB			1	1	Your-image_4096_2160_8.dsc
KGD		~	1	· ·	Click on image to load
		✓ 8 bpc	$\sim$		~
RGB		$\sim$	1	1	
Timing values					
Custom		0			
	H-Total	4400			
	H-Start	216			
	H-Active	4096			
	H-Sync Width	88			
	V-Total	2250			
	V-Start	82			
	V-Active	2160			
	V-Sync Width	10			DSC Status and Configuration
	Frame Rate	60.000			
HK	Sync Negative polarity				C Drable DSC
	Sync Negative polarity				Send PPS
v-sync Negative polarity					Pattern Generator Settings

Select Enable DSC and click Apply.

►

Note	Please note that the output resolution has to match the size of the used compressed DSC image.
Note	Please note that MST and DSC features and cannot be used simultaneously

## Audio Generator Tab

Audio generator allows the user to play LPCM audio generated internally or from files in WAV format.

<u>(</u> iew <u>T</u> ools <u>H</u> elp					
USB-C (Pattern Generator )	Audio Generator Link E		ink DUT Testing \		
Audio Status Audio loaded: 8 channels @ 4	44100 Hz, 16 bits				
Play control Audio from Playing	m: Audio generator.				
Audio Content					
• Generate audio:					
Waveform: Sine	∨ Bits/Sam	ole: 16 bits $\checkmark$			
Signal frequency: 1000	Amplitud	e: 60% ~			
Sample Rate: 4410	00 Hz V Channels	8 Channels V			
O Load audio from file:					
Open WAV file	· · · ·				

To load internally generated audio, select **Generate audio**, and adjust the controls to the desired audio format.

- To load an audio file from your PC, select **Load audio from file**, click the **Open WAV file...** button, browse and select the file and click **Open**
- To play the selected audio content, click the **Play** button.

The content will be looped until the **Stop** • button is clicked.

Audio Status in the top of the tab indicates the type of the currently played audio content.

# Link Tab

Link tab shows the status and control items for the DisplayPort link.

CD-424 [2143C464] - USB-C Source and Sink <u>View</u> <u>Iools</u> <u>Help</u> <u>/USB-C \Pattern Generator \Audio Generator \i</u> HPD Asserted		Sink DUT Testing	\			
Link Status Lane 0 Lane 1 Lane 2 Lane 3 Ci	ock Recovery	Link Configuration Number of Lanes	0	2	٩ (	
	mbol lock nannel equalization	Bit rate, Gbps 0 1.62	0 2.70	0 5.40	06.75	8.10
600         600         600         600         Voltage swing (mVpp)           0         0         0         Pre-emphasis (dB)           0x0000         0x0000         0x0000         Error Count (Click to read)		Additional bit rate	s, Gbps 2.43	03.24	O 4.32	
MST mode: Disabled Framing n FEC status: Disabled DSC statu HDCP status: Disabled SSC Statu	us: Disabled	Downspread Enable SSC Scrambler reset Auto OFFF		Freq (Hz)	31500 ÷	
			💋 Link training		9	Fast LT
Output Level Voltage Swing, mVpp: (© 400 0 600 0 800 1200	Link Pattern Active video Idle Pattern Training Pattern 1		CRC Red CRC: Green CRC:	0x3F3A 0x967D	Сору	
Pre-Emphasis, dB 0	O Training Pattern 1 O Training Pattern 2 O Training Pattern 3		Blue CRC:	0xA7BF		
Apply Overrides     Training Pattern 4     PRBS7     OHBR2 Compliance     SER (Symbol Error     OForce Active Vide     OForce Active Vide			Value 0: Value 1: Value 2:	0x0000 0x0000 0x0000	Сору	

#### HPD

The status LED indicates the state of the HPD signal Asserted (logical "high") or Deasserted (logical "low").

#### Link status

The panel shows the result of the link training with the connected downstream sink and status of connection features.

#### Output Level

Override output level and pre-emphasis values selected during link training. Click **Apply Overrides** to validate changes.

Note Please note that connected Sink and Source actively maintain the link. If the override settings result in link failure, the link will be automatically re-trained and proper values set.

#### Link configuration

Set target capabilities for the link training. Click Link Training to apply.

- Set the Number of Lanes used,
- Set the Link Rate, from standard DP link rates or Additional 'eDP' link rates
- Enable Enhanced Framing Mode
- Force eDP mode. If set, only link rates announced in SUPPORTED_LINK_RATES table (DPCD 00010h 0001Fh) will be used when determining supported link rates.

#### Downspread

Select Enable SSC to enable down spreading of link frequency (SSC).

Set **Amp (‰)** to SSC Spreading Amplitude. Allowed amplitude range is 1 to 10‰ (per mil, 0.1%) (It is mandatory for a DP Rx to support up to 0.5% down spread).

Set Freq (Hz) to SSC Modulation frequency. Allowed Frequency range is 30 to 35 kHz.

#### **Scrambler Reset**

Selection of the value to which the Linear Feedback Shift Register (LFSR) is reset during scrambler reset.

In **Auto** mode UCD verifies that connected DP Sink supports eDP and Alternate Scrambler Seed, and then applies FFFEh. If not, FFFFh will be used.

#### **Fast Link Training**

Click **Fast LT** to initiate a link training without AUX transactions. The procedure will be the following:

- 1. Send idle for  $10 \,\mu s$
- 2. Send TPS1 for 1 ms
- 3. Send TPS2/3/4 for 1 ms
- 4. Send idle for  $10 \,\mu s$
- 5. Send video

#### Link Pattern

Select between Active video and audio, Idle pattern, or special bit patterns.

When **Force Active Video** option is selected, character error messages from sink will not interrupt video transmission.

When **Force Idle Pattern** is selected, Link Training and Active Video will not be initiated even after a re-plug.

Note Please note that except *Active video*, and *Force Active Video* the patterns do not carry video and audio. They are special bit combinations used for development purposes. When selecting **Active Video** (or **Force Active Video**) normal audio and video are being transmitted over the link.

#### CRC

The 16-bit **CRC** (checksum, cyclic redundancy check) values of the three color components calculated by the Sink hardware.

The 16-bit **DSC CRC** values of the captured DSC compressed frame. "**Value 0**" is calculated from  $1^{st}$ ,  $4^{th}$ ,  $7^{th}$  ... byte, "**Value 1**" from  $2^{nd}$ ,  $5^{th}$ ,  $8^{th}$  ... byte and "**Value 2**" from  $3^{rd}$ ,  $6^{th}$ ,  $9^{th}$  ... byte.

# EDID Tab

17	/USB-C \Pattern Generator \Audio Generator \Link \EDID \DPCD \HDCP \FEC \Sink DUT Testir	ng
E	EDID Data:	
Ē	000000 00 ff ff ff ff ff ff 00 54 c7 36 40 4c 34 32 30	EDID Files
	000010 34 18 01 04 e5 3d 23 78 3a 5f b1 a2 57 4f a2 28	Load
	000020 0f 50 54 bf ef 80 71 4f 81 00 81 c0 81 80 a9 c0	Load
	000030 b3 00 95 00 d1 c0 4d d0 00 a0 f0 70 3e 80 30 20	Save as
	000040 35 00 5f 59 21 00 00 1a 56 5e 00 a0 a0 a0 29 50	Jave as
	000050 30 20 35 00 5f 59 21 00 00 1a 00 00 00 fd 00 38	
	000060 4b le 86 36 00 0a 20 20 20 20 20 20 00 00 00 fc	
	000070 00 55 43 44 2d 34 32 34 20 44 50 31 0a 20 01 d8	HEX Editor
	000080 02 03 12 71 83 4f 00 00 29 0f 7f 07 15 06 55 3d	
	000090 lf c0 00 00 00 00 00 00 00 00 00 00 00 00	Clear
	0000a0 00 00 00 00 00 00 00 00 00 00 00	
	00 00 00 00 00 00 00 00 00 00 00 00 00	Append file
	0000c0 00 00 00 00 00 00 00 00 00 00 00	
	0000d0 00 00 00 00 00 00 00 00 00 00 00	
	0000f0 00 00 00 00 00 00 00 00 00 00 00	EDID Editor
		Virtual Channel 3 Connected Sink EDID Read
		кеаа

EDID tab enables analyzing and saving the EDID read from the connected Sink device.

There are three basic functions:

- Read the contents of the EDID of the downstream sink over the DisplayPort link.
- Load and save EDID data files in the host PC
- Edit the EDID contents

#### **EDID Files**

Note

With **Load...** and **Save as...** a hex EDID file can be read and written from the PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

Four blocks (512 bytes) of EDID code is read. If the device is not supporting all four blocks, the non-supported area is replaced with zeroes.

Currently the EDID Editor does not support Display ID. Hex EDID files can however be modified with the HEX Editor or externally generated hex EDID files that have Display ID content can be load and programmed into the hardware.

#### **HEX Editor**

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. EDID contents can be edited by typing over the existing values. Altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

After editing the data can either be saved to an *.ecd file in the PC with **Save as...** or programmed it to the hardware EDID memory with **Write**.



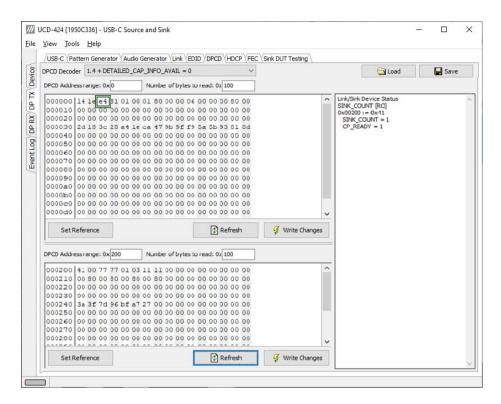
#### **EDID Editor**

EDID Editor is launched in a separate pop-up window. Please see the description of the EDID editor in Chapter <u>EDID Editor</u> later in this document.

DID Editor			-	×
EDID Editor         E-EDID Encoder / Decoder <ul> <li>Blocks in collection</li> <li>Blocks (PESA EDID)</li> <li>Checksum</li> <li>Version</li> <li>Extension flag</li> <li>Verdori &amp; Product ID</li> <li>Basic Display Parameters and Feab</li> <li>Display x,y Chromacity coordinatee</li> <li>Established timings I and II</li> <li>Standard Timings</li> <li>Standard Timings<!--</td--><td>Details of ":/0/Version/Vendor Product ID Key ID Manufacturer Name ID Product Code ID Serial Number Manufacture or Model year Week of manufacture Year of manufacture</td><td>Value UFG 0x4036 0x3032344c Manufacture Year and Week Week 52 Year 2014</td><td>_</td><td>×</td></li></ul>	Details of ":/0/Version/Vendor Product ID Key ID Manufacturer Name ID Product Code ID Serial Number Manufacture or Model year Week of manufacture Year of manufacture	Value UFG 0x4036 0x3032344c Manufacture Year and Week Week 52 Year 2014	_	×
Checksum CEA Extensions Version Sink Underscans IT video Basic audio YCbCr (4:4:4) YCbCr (4:2:2) Native DTD's in entire E-EDID 18-Byte Descriptors in this block CEA Data block count Load Load Save Save Save	Constant Show Log			

# DPCD Tab

DPCD tab is a tool for monitoring and editing the DPCD registers of the connected Downstream Sink.



The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

In the combo box above the DPCD Decoder window you can select how the DPCD data is interpreted, either as *DP 1.1 DPCD*, or as *DP 1.2 DPCD* with *Detailed Capability Info* selected or not (DETAILED_CAP_INFO_AVAIL = 1/0).

By clicking **Refresh** you can re-read the data from the DPCD registers to the window in question.

By clicking **Write Changes** you can write the portion of data shown in the window in question to the DPCD registers.

By clicking **Set Reference** you can store currently shown data as a reference for comparison.

When you refresh the data from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with **red** color.

/USB-C \Pattern General	tor \Audio Generator \Link \ED		k DUT Testing		
DPCD Decoder 1.4 + DE	TAILED_CAP_INFO_AVAIL = 0	~		🔄 Load	🔒 Save
DPCD Address range: 0x	0 Number of bytes	to read: 0x 100			
000010         00         00         00           000020         00         00         00           000030         24         18         32           000040         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00           000050         00         00         00	$ \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 8 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	LANEO 0X002 LANE LANE LANE LANE LANE	ki: Device Status 1. STATUS [RO] 22:=0X77 30: CR.DONE = 1 30: CRIANNEL_EQ_DONE = 1 30: CRIANNEL_EQ_DONE = 1 1: CR.DONE = 1 1: CRIANEL_EQ_DONE = 1 1: CRIANEL_EQ_DONE = 1 1: SYMBOL_LOOKED = 1	
DPCD Address range: 0x	200 Number of bytes	to read: 0x 100			
000210 00 80 00 000220 00 00 00 000230 00 00 00 000240 3a 3f 7d 000250 00 00 00 000260 00 00 00	77 80 03 11 11 00 00 00 80 00 80 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00	0 00 00 00 00 00 00 0 00 00 00 00 00 00 0 00 0			

### Saving and Loading DPCD Content

DPCD data in the selected address areas can be saved as a file in your PC. There are three alternative formats:

- Binary *DPCD Fata File* format (*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- Comma Separated Values (*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (*.HEX) in a human readable text format.
- Click **Save** to select the location and the format of the file.
- Click Load to load DPCD data saved in *DPCD Data File* (*.DPD) format to the editor.
- To program the data into the DPCD registers of UCD-424 Local Sink click Write Changes.

Note	- Writing DPCD data to the DPCD registers of the Sink will potentially affect the
	status and capabilities of sink as seen by the source. - User control like Link Training or mode changes will modify the content of the
	DPCD registers

# HDCP Tab

HDCP tab is the dialog for monitoring the HDCP (for *High-Bandwith Digital Content Protection*) status and controlling the HDCP capabilities of the connected UCD-424 device.

HDCP 1.3 Status	Active Authenticated Authenticated Keys loaded	nk VEDID VEPCD VHDCP VFEC (Sink D Configuration Enable encryption Authenticate Keys @ Production O Facsimile - "Test" None			
HDCP 2.3 Status	Active Authenticated Authentication in progress Keys loaded	Configuration Configuration Authenticate Keys Production Facsimile - "Test" - R1 Facsimile - "Test" - R2 None	Content level Type 0 Type 1		

#### Status

The status fields indicate the HDCP status of the connected UCD-424 device.

Active: The stream between UCD-424 and the downstream sink has been encrypted.

*Authenticated*: The HDCP handshake between the UCD-424 and the sink unit has been completed successfully.

Authentication in process: The HDCP handshake is in process between the UCD-424 and the downstream sink unit.

Keys loaded: The HDCP keys are loaded to the UCD-424 unit.

#### Configuration

*Enable encryption*: Check to enable the encryption of the stream between UCD-424 and the downstream sink.

*Authenticate*: Perform the HDCP initiation handshake between the UCD-424 and the sink unit.

#### Keys

Select between Production or Facsimile HDCP keys. To remove the keys, select None.

#### **Content level**

Selection of Type 1 content ensures that content encryption is done with HDCP version 2.2 or higher.

#### HDCP 1.3 vs. HDCP 2.3

UCD-424 devices support by default HDCP 1.3 and HDCP 2.3.

# FEC Tab

Forward Error Correction (FEC) can be enabled if connected sink supports it. For debug purposes, error injection to main-link is possible. There is an error type for each standard sink DPCD error counter.

File       View       Jools       Help         UBR-C (Pattern Generator \Audo Generator \Link \EDID \DPCD \HDCP) FEC \Sink DUT Testing       FEC         FEC       FEC Enabled       Prefer FEC Enabled       Enable FEC       © Deable FEC         From generator       Number of errors to generate for Lane #0:       0       0       FEC Status Log         Number of errors to generate for Lane #1:       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0		CD-424 [1950C336] - USB-C So	ource and Sinl	k				-		×	
Number of errors to generate for Lane #0:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #2:       0       ↓         Number of errors to generate for Lane #3:       0       ↓         Generate errors of type:       Corrected parity 1 error       ↓         Delay between steps (in microseconds):       100       ↓         Incorrected block errors       0       0       0         Uncorrected block errors       0       0       0         Parity block errors       0       0       0         Petug FEC Sequence       Image for the for the for the fort th	_	/USB-C \Pattern Generator \Au	udio Generator			CP FEC Sink	DUT Testing \				
Number of errors to generate for Lane #0:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #2:       0       ↓         Number of errors to generate for Lane #3:       0       ↓         Generate errors of type:       Corrected parity 1 error       ↓         Delay between steps (in microseconds):       100       ↓         Incorrected block errors       0       0       0         Uncorrected block errors       0       0       0         Parity block errors       0       0       0         Petug FEC Sequence       Image for the for the for the fort th	Devi	FEC Enabled	Prefer FEC E	Enabled		Enable FEC	Disable FEC				
Number of errors to generate for Lane #0:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #1:       0       ↓         Number of errors to generate for Lane #2:       0       ↓         Number of errors to generate for Lane #3:       0       ↓         Generate errors of type:       Corrected parity 1 error       ↓         Delay between steps (in microseconds):       100       ↓         Incorrected block errors       0       0       0         Uncorrected block errors       0       0       0         Parity block errors       0       0       0         Petug FEC Sequence       Image for the for the for the fort th	E E	Error generator					FEC Status Log				
Number of errors to generate for Lane #2:       0       ◆         Number of errors to generate for Lane #3:       0       ◆         Generate errors of type:       Corrected parity 1 error       ●         Delay between steps (n microseconds):       100       ◆         Sink Error Counters (DPCD)       Iane #0       Lane #1       Lane #2       Lane #3         Uncorrected block errors       0       0       0       0         Disterrors       0       0       0       0         Parity block errors       0       0       0       0         Debug FEC Sequencing        Send FEC Enable Sequence       Clear Ion	RX C	Number of errors to generat	e for Lane #0:		0	•		equence N	OT detect	ed	
Generate errors of type:       Corrected parity 1 error         Delay between steps (in microseconds):       100         Image: Ima	B	Number of errors to generat	e for Lane #1:		0						
Generate errors of type:       Corrected parity 1 error         Delay between steps (in microseconds):       100         Image: Ima	Do										
Generate errors of type:       Corrected parity 1 error         Delay between steps (in microseconds):       100         It corrected block errors       0         Uncorrected block errors       0         0       0         Corrected block errors       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0       0         0	Trent										
Delay between steps (in microseconds):       Ito         Image: Imag	5	Generate errors of type:		Corre	cted parity 1	Lerror V					
Sink Error Counters (DPCD) Lane #0 Lane #1 Lane #2 Lane #3 Corrected block errors 0 0 0 0 Bit errors 0 0 0 0 0 Bit errors 0 0 0 0 0 Parity block errors 0 0 0 0 0 Parity block errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Delay between steps (in mic	roseconds):		100	-					
Lane #0       Lane #1       Lane #2       Lane #3         Uncorrected block errors       0       0       0         Corrected block errors       0       0       0         Bit errors       0       0       0         Parity block errors       0       0       0         Parity bit errors       0       0       0         Ø Update  Ø Clear counters           Debug FEC Sequencing              Send FEC Enable Sequence					💋 Ap	ply					
Uncorrected block errors 0 0 0 0 0 Corrected block errors 0 0 0 0 0 Bit errors 0 0 0 0 0 Parity block errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 0 0 0 Parity bit errors 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Sink Error Counters (DPCD)									
Corrected block errors         0         0         0           Bit errors         0         0         0           Parity block errors         0         0         0           Parity bit errors         0         0         0           Parity bit errors         0         0         0           Ø Update         Ø Clear counters           Debug FEC Sequencing           ◆ Send FEC Enable Sequence         ✓ Send FEC Disable Sequence			Lane #0	Lane #1	Lane #2	Lane #3					
Bit errors       0       0       0         Parity block errors       0       0       0         Parity bit errors       0       0       0         Image: Im			-			-					
Parity block errors       0       0       0         Parity bit errors       0       0       0         ✓ Update       ✓ Clear counters         Debug FEC Sequencing         ▲ Send FEC Enable Sequence       ◆ Send FEC Disable Sequence			-			-					
Parity bit errors       0       0       0         Image: I					-	•					
Debug FEC Sequencing   Send FEC Enable Sequence    Clear Inn						•					
Send FEC Enable Sequence		3	<b>U</b> pdate		💋 Clear co	ounters					
Clear lon		Debug FEC Sequencing									
Sink FEC Status: Decode Enable Detected		Send FEC Enable Seq	uence	🗣 Send	FEC Disable	Sequence					
		Sink FEC Status: Decode Enable	Detected				Clear log				
		_									

#### FEC

Clicking **Enable FEC** UCD-424 will verify if connected sink supports FEC and begins the handshake for enabling FEC.

Clicking **Disable FEC** UCD-424 will start the FEC disable handshake.

If **Prefer FEC Enabled** is selected and the connected sink supports FEC, UCD-424 will start the FEC Enable Sequence after a successful connection.

#### **Error Generator**

Generate errors of type: selection will set how many errors will be inserted into one FEC block and to which link symbols. There are five options:

- Uncorrected block: 3 symbol errors with 3 error bits together
- Corrected block: 2 symbol errors with 2 error bits together
- Corrected parity: 2 parity byte errors with 2 error bits together
- Corrected block 1 error
- Corrected parity 1 error

Note: FEC must be enabled and running before errors can be added.

Each lane can have its individual error amount. Errors can be injected to even and odd decoders by using **lane #0** and **lane #1** counters when link is configured to one lane.

Clicking Apply will start error injection.

Clicking Update will read sink DPCD FEC error counter registers.

Clicking Clear counters will clear sink DPCD FEC error counter registers.

Note: Link training will reset sink FEC error counters.

#### Debug FEC Sequencing

When clicking **Send FEC Enable Sequence** UCD-424 will start adding *FEC Enable Sequence* in its main link data.

When clicking **Send FEC Disable Sequence**, UCD-424 will start adding *FEC Disable Sequence* in its main link data.

## Sink DUT Testing Tab

Please refer to **Appendix E** later in this document for description of the tests available. Sink DUT Testing enables the execution of HDCP 2.3 Compliance Tests for a DP Sink DUT. Sink DUT Testing enables testing of a DP Sink DUT. Please refer to **Appendix E** of this document to get a full definition of the Test Cases and test parameters.

100 UCD-424 [1950C336] - USB-C Source and Sink		-	_		×
<u>Eile View T</u> ools <u>H</u> elp					
/USB-C \Pattern Generator \Audio Generator \Link \EDID \DPCD \HDCP \FEC \Sink DUT Testing					
Unk-Layer Tests V HDCP 2.3 2C tests V HDCP 2.3 3C tests					
Test Name	Pass	Fail	Skip	Run	^
A 5.2.1.1 Read One Byte from Valid DPCD Address	1	0	0	1	
☑ ✓ 5.2.1.2 DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	1	0	0	1	
▲ 5.2.1.3 Write One Byte to Valid DPCD Address	1	0	0	1	
S 5.2.1.4 Write Nine Bytes to Valid DPCD Addresses	1	0	0	1	
S.2.1.4 Write Nine Bytes to Valid DPCD Addresses     S.2.1.5 Write EDID Offset (One Byte 12C-Over-AUX Write)     S.2.1.5 Write EDID Offset (One Byte 12C-Over-AUX Write)	1	0	0	1	
5.2. 1.6 Read One EDID Byte (One Byte I2C-Over-AUX Read)	1	0	0	1	
🖌 5.2.1.7 EDID Read (1 Byte I2C -Over-AUX Segment Write, 1 Byte I2C-Over-AUX Offset Write, 128 Byte I2C-Over-AU	1	0	0	1	
🖌 5.2. 1.8 Illegal AUX Request Syntax	1	0	0	1	
5.2.1.9 Gitch Rejection	1	0	0	1	
5.2.1.10 Interleaved EDID and DPCD Receiver Capability Read	0	0	0	0	
- 5.2.1.11 Downstream Stop on MOT Reset	0	0	0	0	
<ul> <li>5.2.1.12 Downstream Stop on Timeout</li> </ul>	0	0	0	0	~
🗎 Configure	Impo	rt	Ľ	Export	t
Run Selected Stop on Failure Repeats: 1 🗘 Delay time, sec: 1 🗘 Save Report			Cle	ar All	
Test Log:					
<pre>0000.102.392: Reference Source enabled its AUX receive logic, waits for lms, and verifi does not send a reply. 0000.103.615: No AUX channel reply is detected. 0000.103.519: Test PASSED: "5.2.1.5 Glitch Rejection" *** Test complete PASSED ***</pre>	es th	at th	e Sin	k DUT	^
lest complete PASSL					~

Select the tests for execution by clicking the corresponding row.

Clicking **Configure...** opens a dialog for defining the test parameters for that set. Please refer to *Test Parameters* below for description.

Parameters from Test descriptor files can be loaded with **Import** and stored with **Export**. Please refer to chapter *Exporting Tests for TSI* later in this document.

Tests are started by clicking Run Selected. By clicking Abort the sequence is stopped.

Test flow can be controlled with **Repeats** of the test sequence, **Delay** between individual tests or **Stop on Failure** that stops the whole sequence if one of the tests fail.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

Click **Save Report** to generate a HTML report file for sharing the results with other parties for viewing without UCD Console.

By clicking Clear All the test log and the results matrix are cleared.

### **Test Parameters**

Each test set has its dedicated set of test parameters. To open a dialog for defining the parameters click **Configure...** 

#### Parameters of LL CTS Tests

Link-Layer Tests parameter panel defines which resolutions and video modes are used for testing.

They can be defined in the matrix in the dialog by selecting **Use test configuration (below)** or determined by evaluating content of DUT EDID by selecting **Use sink DUT EDID**.

DP 1.4 LL CTS DUT Sink Ca	apabilities			_		×
Test Parameters						
Test timeout, milliseconds	10000	Most packed video mode(s)	Use sink DL	JT EDID		$\sim$
DSC video mode(6) 1920 x 1080 @ 30 Hz 1920 x 1080 @ 60 Hz 1920 x 1080 @ 120 Hz 3840 x 2160 @ 30 Hz 3840 x 2160 @ 60 Hz 3840 x 2160 @ 120 Hz 5120 x 2160 @ 30 Hz 5120 x 2160 @ 60 Hz 5120 x 2160 @ 120 Hz 7680 x 4320 @ 30 Hz 7680 x 4320 @ 60 Hz 7680 x 4320 @ 100 Hz	Use test configuration (below)         ✓           CTA         RB1         RB2           □         □         □           ∅         □         □           ∅         □         □           ∅         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □           □         □         □	Ilane           UVT 1280 x 800 @ 60p [R81]           DMT 1280 x 768 @ 60p [R81]           DMT 1280 x 768 @ 60p 18bp           CTA 1440 x 480 @ 539.94p 24           CTA 1440 x 766 @ 60p 18bp           DMT 1024 x 766 @ 50p 24bp           DMT 1280 x 1024 @ 60p 24bp           DMT 1280 x 1024 @ 60p 24bp           DMT 1280 x 960 @ 60p 30bpp           DMT 1280 x 300 @ 60p 30bpp           DMT 1400 x 1050 @ 60p [R8           DMT 1280 x 768 @ 60p 30bpp           CVT 1280 x 800 @ 60p 30bpp           DMT 1400 x 1050 @ 60p [R8           DMT 1280 x 768 @ 60p 30bpp           CVT 1280 x 768 @ 60p 30bpp           DVT 1600 x 1200 @ 60p [R8]	<pre>1 18bpp 95% 2)bpp 93% p 90% 8pp 100% p 100% p 100% p 100% p 99% p 97% 1] 24bpp 94% p 92%</pre>	6		
Display ID Visual Checks DSC Simple 422 CRC	Set / Clear All Never skip  YCbCr 444 bitstream  V	4 lanes CVT 2048 x 1536 @ 60p [RB1 DMT 1792 x 1344 @ 60p 24b DMT 1600 x 1200 @ 60p 30b CTA 1920 x 1080 @ 60p 30b;	pp 95% pp 94%			
Presets		✓ 0	ж	×	Cancel	

#### Parameters of HDCP CTS Tests

HDCP CTS Tests have their own parameter dialog.

DP HDCP CTS 2C test parameters			-		×
Test Parameters					
Test timeout, milliseconds	100000				
2 L.					
Presets	🗸 o	к	2	🕻 Cancel	

#### **Saving and Loading Presets**

In all parameter dialogs the selected parameters can be saved as Presets. Please click **Presets...** to save or recall a configuration.

### Exporting Tests for TSI

Unigraf UCD Console includes a feature rich Software Development Kit (SDK) for use in automated testing. The SDK is called Test Software Interface (TSI). TSI allows for an easy integration of Production and R&D testing routines into an automated test system environment. Please refer to TSI documentation found in additional Unigraf manuals for details.

The tests included in UCD Console's Source DUT Testing tab and Sink DUT Testing tab can be executed in TSI environment. A straightforward way is to use UCD Console's *Tools* > *TSI Integration* dialog to create the necessary files for TSI environment and use *Export* function in *DUT Testing* tabs to include the intended tests.

	Configure	Ľ	Imp	ort		Expor	t
<ul> <li>5.2.1.12 Downstream Stop on Timeout</li> </ul>			0	0	0	0	
<ul> <li>5.2.1.11 Downstream Stop on MOT Reset</li> </ul>			0	0	0	0	
5.2.1.10 Interleaved EDID and DPCD Receiver Capability Read			0	0	0	0	
5.2.1.9 Glitch Rejection			1	0	0	1	_

*Export:* Save parameters of the selected test to a file. If TSI Integration is enabled in Tools > Options, also the test is appended into 'Run Test' file in TSI workspace folder.

*Import:* Recall parameters from configuration file. If TSI Integration is enabled in Tools > Options, parameters are imported from a file in TSI workspace folder

# 8. COMPLIANCE TESTS

Compliance test capability is a license enabled add-on to UCD Console.

The tests are included in the GUI software, license codes enable the tests for use. Please refer to *Appendix B Licensing* for details. The list of compliance tests that UCD Console supports, please refer to document *DP CTS Tool Options for Unigraf UCD-400.pdf*. It can be downloaded in Unigraf Documents at <u>https://www.unigraf.fi/documents/</u> If you have any additional questions, please contact Unigraf or your local representative.

Compliance tests (CTS Tests) are part of tests included in **Source DUT Testing** tab of **DP RX** and **Sink DUT Testing** tab of **DP TX**.

IVID         UCD-424 [1950C336] - USB-C Source and Sink           Eile         View         Tools           Help		-	-		×
/USB-C \Pattern Generator \Audio Generator \Link \EDID \DPCD \HDCP \FEC \Sink DUT Testing \					
Bit         / Link-Layer Tests         \ HDCP 2.3 2C tests         \ HDCP 2.3 3C tests					
Test Name	Pass	Fail	Skip	Run	^
△ 5.2.1.1 Read One Byte from Valid DPCD Address	1	0	0	1	
✓ 5.2.1.2 DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	1	0	0	1	
△ S.2.1.3 Write One Byte to Valid DPCD Address	1	0	0	1	
5.2.1.4 Write Nine Bytes to Valid DPCD Addresses	1	0	0	1	
S.2.1.4 Write Nine Bytes to Valid DPCD Addresses     S.2.1.5 Write EDID Offset (One Byte 12C-Over-AUX Write)     S.2.1.5 Write EDID Offset (One Byte 12C-Over-AUX Write)	1	0	0	1	
V 5.2.1.6 Read One EDID Byte (One Byte I2C-Over-AUX Read)	1	0	0	1	
🖌 5.2.1.7 EDID Read (1 Byte I2C -Over-AUX Segment Write, 1 Byte I2C-Over-AUX Offset Write, 128 Byte I2C-Over-AU	1	0	0	1	
5.2.1.8 Illegal AUX Request Syntax	1	0	0	1	
5.2.1.9 Glitch Rejection	1	0	0	1	
5.2.1.10 Interleaved EDID and DPCD Receiver Capability Read	0	0	0	0	
<ul> <li>5.2.1.11 Downstream Stop on MOT Reset</li> </ul>	0	0	0	0	
<ul> <li>5.2.1.12 Downstream Stop on Timeout</li> </ul>	0	0	0	0	~
E Configure	Impor	rt	Ľ	Export	
Run Selected Stop on Failure Repeats: 1 + Delay time, sec: 1 - Save Report			Clea	ar All	
Test Log:					
0000.102.392: Reference Source enabled its AUX receive logic, waits for lms, and verifidoes not send a reply.	es tha	at th	e Sin	k DUT	^
0000.103.615: No AUX channel reply is detected.					
0000.103.919: Test PASSED: "5.2.1.9 Glitch Rejection"					
*** Test complete PASSED ***					
					~

The tests cases are divided to test categories as described in *Appendix E* of this document. Each test category can be found in its dedicated sub-tab. The sub-tabs as in turn enabled by the licenses present in user's PC. Please refer to chapter 3 *License Manager* earlier in this document.

### **DSC Test Content**

When running DSC Compliance Tests, UCD-424 needs to have access to DSC content used as test patterns. The content can be created from the source bitmap files downloaded during installation (optional) either with Unigraf DSC Content Creator or created by the Compliance Test Tool on-the-fly during the compliance test.

#### Options

In Tools > Options menu you can define DSC Work folder DSC test content directory.

You can also select to *Automatically create missing content*, automatically create the DSC compressed content used for testing the DUT. You can also *Keep auto-created DSC content files:* By default, the DSC compressed content is deleted after use. If selected, the content is not kept, not deleted.

Warning Keeping the automatically created DSC compressed content will shorten the time needed for running the DSC compliance tests.

Please note, that the space needed for storing the full library **can be very large** (appr. 200 GBytes). Please make sure that the content will be stored in a medium that has the required space available.

### Test Parameters

Before running the tests, capabilities of the DUT have to be defined for the test engine. Each test category has its dedicated test parameter dialog. Click **Configure...** in *Source DUT Testing* or *Sink DUT Testing* tab to open the parameter dialog.

	aptiveSync							
Test timeouts		Colorimet	try					
Fest timeout (milliseconds):	5000	*	RGB		YCbCr 4:2:2		YCbCr 4:4:4	
ong HPD pulse duration (milliseconds):	1000	6bpc V	VESA	🗌 8b	pc CTA (ITU.601)		8bpc CTA (ITU.601)	
T Start timeout (milliseconds):	5000	8bpc V	VESA	10	bpc CTA (ITU.601)		10bpc CTA (ITU.601)	
Fest cycle delay (milliseconds):	5000	🔺 🗌 10bpc		_	pc CTA (ITU. 709)	_	8bpc CTA (ITU.709)	
DUT Capabilities				10	bpc CTA (ITU. 709)		10bpc CTA (ITU. 709)	
Max lanes supported:	4Lanes	10bpc	: CTA					
Max bit rate supported:	HBR3 (8.10 Gbps)	Select	t All					
Voltage Swing level 3 (1.2V) supporte		Video Mo	des					
Pre-Emphasis level 3 (9.5dB) supporte	d		video mode:					
Fixed timing DUT					640x480 @ 60Hz 6 B			
Spread Spectrum Supported		Maximum	supported video m	ode:	3840x2160 @ 60Hz 8	3 BPC		$\sim$
Video format change without LT suppo	rted	Most Par	ked Timings					
Lane count reduction without LT supp	orted		-					
✓ E-DDC supported		1 Lane	CTA 1440 x 576p	-				~
Audio Info Frame supported for 2 cha	nnel audio	2 Lanes	CVT 1600 x 1200	p @ 60	Hz, RB1, 6 bpc			$\sim$
DUT is Type-C Device		4 Lanes	CVT 2048 x 1536	p @ 60	Hz, RB1, 8 bpc			$\sim$
FEC supported		Time-sta	mp generation					
FEC disable sequence supported		Time Star	1 Jane		2 Lanes		41 anes	
Audio without Video supported		RBR	848x480@60 Hz	~	1280x720@60 Hz	~	1920×1080@60 Hz	$\sim$
Test Automation TEST_LINK_TRAINING		HBR	1280x720@60 Hz		1280x960@60 Hz	~	1920x1080@60 Hz	
TEST_EDID_READ								~
TEST VIDEO PATTERN		HBR2	1280x960@60 Hz		1920x1080@60 Hz		1920x1080@120 Hz	~
TEST_AUDIO_PATTERN		HBR3	1920x1440@60H	z v	3840x2160@30Hz	~	3840×2160@60Hz	~
Event indicating DUT ready:	Active Video	~						

For a detailed description of capabilities listed on the tab please refer to *Chapter 3 Compliance Test Operation* of document *VESA DisplayPort v1.4a Link Layer Compliance Test Specification*.

Note Please make sure that the capability tables are completed before running the tests. The result of the test might be misleading if the DUT capabilities and the table do not match.

### **Saving Test Parameters**

Test parameters can be saved for later use in two ways: internally or externally in a file.

In parameter dialog the parameter set can be saved as an internal Preset.

In *Source* or *Sink DUT Testing* tab **Export** saves test definitions of each selected test in a separate file. **Import** loads the parameters back to UCD Console. They can be run with Unigraf TSI. Please refer to chapter *7.3.6 Running Tests* in document *TSI-X_Reference.pdf* in UCD Console release package.

# **Running CTS Tests**

*Source DUT Testing* and *Sink DUT Testing* tabs include the tests enabled with the set of licenses present in UCD Console. The tests are grouped in test set tabs. In tabs the tests are listed by the test name and reference number as presented in applicable compliance test specification. UCD-424 firmware implements the test according to the test specification.

For running a test, select it and click **Run selected**. For selecting multiple consecutive tests in the list hold down the **Shift** key of your keyboard while selecting the tests. For selecting multiple individual tests hold down the **Ctrl** key in your keyboard while selecting.

	UCD-424 [1950C336] - USB-C Source and Sink View Tools Help		-	-		×
	/USB-C \Pattern Generator \Audio Generator \Link \EDID \DPCD \HDCP \FEC \Sink DUT Testing \					
8						
Device	Link-Layer Tests V HDCP 2.3 1A tests V HDCP 2.3 1B tests V HDCP 2.3 3A tests V HDCP 2.3 3B tests V CRC tests	Simp	ole LT te	ests \		
Ĕ	Test Name	Pass	Fail	Skip	Run	^
B	4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	0	0	0	0	
RX	4.2.1.2 Source Retry on Invalid Reply During AUX Read after HPD Plug Event	0	0	0	0	
Event Log DP	4.2.1.3 Source Device HPD Event Pulse Length Test	0	0	0	0	
2 S	4.2.1.4 Source Device IRQ_HPD Pulse Length Test	0	0	0	0	
ent	<ul> <li>4.2.1.5 Source Device Inactive HPD / Inactive AUX Test</li> </ul>	0	0	0	0	
Ē	<ul> <li>4.2.2.1 DPCD Receiver Capability and EDID Read upon HPD Plug Event</li> </ul>	0	0	0	0	
	<ul> <li>4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event</li> </ul>	0	0	0	0	
	- 4.2.2.3 EDID Read	0	0	0	0	
	– 4.2.2.4 EDID Read Failure #1: I2C-Over-AUX NACK	0	0	0	0	
	<ul> <li>4.2.2.5 EDID Read Failure #2: I2C-Over-AUX DEFER</li> </ul>	0	0	0	0	
	<ul> <li>4.2.2.6 EDID Corruption Detection</li> </ul>	0	0	0	0	
	<ul> <li>4.2.2.7 Branch Device Detection upon HPD Plug Event</li> </ul>	0	0	0	0	~
	달 Configure [[	Impo	rt	Ľ	Export	t
	Run Selected Stop on Failure Repeats: 1 + Delay time, sec: 1 + Save Report			Cle	ar All	
	Test Log:					
						^
						~

**Repeats** defines number of test-runs and the **Delay time** delay between the tests. When repeating a sequence of tests, all selected tests are performed in each repetition. E.g. when you repeat tests 1, 2 and 3 two times, the sequence is: 1, 2, 3, 1, 2, 3.

Test flow parameters like **Test timeout** and **Test cycle delay** can be defined in *Test Parameter* dialog launched by clicking **Configure...**.

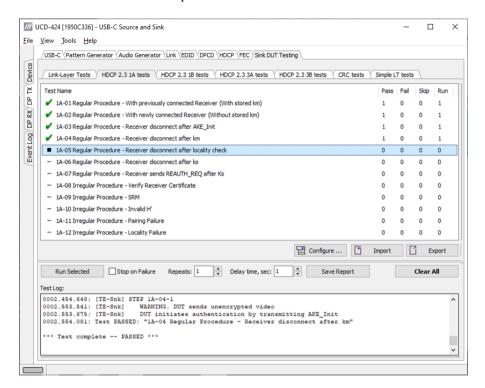
Selecting Stop on Failure stops execution of a series of tests in case a failure is found.

For clearing the Status Log and the Results matrix, click Clear All.

### **Evaluating CTS Test Results**

The test procedure advancement can be monitored in the *Test Log* panel. It describes the steps of each individual test in the way defined in the corresponding VESA Compliance Test Specification. Please use the Status Log and Specification side by side when interpreting the results.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.



# Test Report

Results of the test can be saved as a report in HTML format.

Click **Save Report** in UCD Console. A dialog will open where information about the DUT and remarks about the test can be included in the report. Details of the used test equipment and the software and firmware version will be added automatically.

/// Report information	- 🗆 X
JCD-400 [1924C312]         DUT Information           Serial number:         Model:           1924C312         ABC           Firmware package:         Model:           MN 1.8.11 MF 1.7.9         Eastername           Application Version         XX           Version 1.9 [R0], Build# 25582         Firmware version:           Driver:         Driver:           Tested by:         Tester	DUT Information
Serial number:	
1924C312	ABC
Firmware package:	
MN 1.8.11 MF 1.7.9	1234567890
	DUT Information           Model:           ABC           Serial Number:           1234567890            Revision:           IX           Firmware version:
Version 1.9 [KU], Build# 25582	Firmware version:
	Driver:
Report Information	
Tested by: Tester	
Remarks: (1024 chars max.)	
	🖌 Save 🕺 K Cancel

### Viewing the CTS Test Report

The report file can be viewed with any HTML browser. The report has built-in views for Report Summary, Test Summary and individual Test Logs.

Unigraf Test Report	× +		-	
) → C' û	Q file:///C:/Users/aaa/Desktop/test.html	<u>*</u>	\ ⊡	۲
Total number of test runs Passed test runs: 4 Failed test runs: 0 Skipped test runs: 0 Aborted test runs: 0	4			
EST DETAILS, TEST 1				_
,	ure - With previously connected Receiver (With stored km)			
Test Result: PASSED				
Test Settings: Test timeout, millisecond Revoke ID = 71.6A.15.46 Source_EncDisableBoo	BF			
Test Log				
0000.000.1466 [TE: 0000.000.256; [TE: 0011.000.9166 [TE: 0011.001.250; [TE: 0011.001.250; [TE: 0011.001.250; [TE: 0011.100.0211; [TE: 0011.255.917; [TE: 0011.255.917; [TE: 0012.254.170; [TE: 0012.254.100; [TE: 0012.254.100; [TE: 0012.254.100; [TE: 0012.254.100; [TE: 0012.254.100; [TE: 0012.254.100; [TE: 0012.244.100; [TE: 0012.244.100	hk] TE transmits Receiver Connected Indication(Hot plug, CONNECTION_STATUS hk] [Authentication and Key Exchange] hk] STEP 1A-01-2 hk] WARNING, DUT sends unencrypted video hk] DUT initistes authentication by transmitting AKE_Init hk] AKE_Send_Cert message is available hk] DE Sends AKE Song Sotored km message hk] Send AKE Send pairing_Info message hk] Send AKE Send pairing Info message hk] Step 1A-01-4 hk] DUT sends Lo_Init message hk] Step 1A-01-4 hk] DUT sends SE Send Ex message hk] Step 1A-01-6 hk] DUT enables HDCP enurption hk] STEP 1A-01-7 hk] Checking the correctness of the LINK VERIFICATION_PATTERN within the f hk] Authentication and link integrity check complete PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "A-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With previously connected Receiver (With s PASSED: "IA-01 Regular Procedure - With Previously connected Receiver (With s PA	5_NOTIFY and IRQ_	-	on
EST DETAILS, TEST 2				
1A-02 Regular Proce	ure - With newly connected Receiver (Without stored km)			
Test Result: PASSED				

# 9. EVENT LOG

*Event Logger* (Event Log) vertical tab can be seen on the left edge of the GUI. Event Log is enabled with UCD Pro for DP Sink or UCD Pro for DP Source license.

Event Log dialog is divided into two panels: the left panel lists all transactions, and the right panel shows the parsed transaction data for the line selected in the list on the left.

Start Capture	I S	top Capt	ure					
Start Capture Data sources and filters:		/Event	Log (DP AU)	( analyzer	(DP Out	put po	ort) \DP AUX analyzer (DP Input port) \	
DisplayPort Output     HPD			<u>S</u> ave	🖹 Re	port	(	Open	
AUX     UX     DisplayPort Input     PHPD     VHPD     VAUX     SOP     VIDA changes     VUB-C DPRX     VIB-C DPRX     VSB-C DPTX     DSB-C DPTX     DPD	٨	# 7 8 9 10 11 12 13 14 15 16 17 18 19	Timesta 11115 11115 11115 11115 11115 11115 11115 11115 11115 11115 11115	Type MSAx VB-IDx MSAx VB-IDx USB-C USB-C VB-IDx VB-IDx VB-IDx VB-IDx VB-IDx VB-IDx USB-C	From	F 2 3 3 0 0 2 3 1 1 0 7 0	Data 1916x1080 (HT 2200, VT 1125, HS 192, VS 41,. 1920x1080 (HT 2200, VT 1125, HS 192, VS 41,. (SNK){3}: (VDM) (SRC}3): (GOOD CRC} HPD High, Cable Connected, Power present (SNK){4}: (VDM)	24: 111157309.398ms Device ID: 01 (DisplayPort RX) Flags: 0 (Data message) Direction: Sink to Source Native AUX Reply: AUX_ACK IZC-over-AUX Reply AUX_ACK Data: [≢24] 00 80
		20 21 22 23 24 25 26 27 28 29 30	11115 11115 11115 11115 11115 11115 11115 11115 11115 11115 11115 11115	USB-C AUX AUX AUX AUX AUX AUX AUX AUX AUX AUX		0 8 0 8 0 8 0 8 0 8 0 8	(SRC) {4}:{GOOD CRC} Address: 0x000201 Native AUX Request Comm. Native AUX Reply: AUX_ACK; Address: 0x00000E Native AUX Request Comm. Native AUX Reply: AUX_ACK; Address: 0x002200 Native AUX Request Comm. Native AUX Reply: AUX_ACK; Address: 0x0F0000 Native AUX Request Comm. Native AUX Reply: AUX_ACK; Address: 0x000201 Native AUX Request Comm. Native AUX Reply: AUX_ACK;	

With the Event Logger captures the following items

- HPD status (DP TX and DP RX)
- AUX transaction (DP TX and DP RX)
- DP SDP messages (DP RX)
- Changes in MSA (DP RX)
- Changes in VB-ID (DP RX)
- USB-C PD transaction

Each item line includes Time stamp, Type indication, Message source, and raw message data. The right panel lists the content of one message. Messages belonging together with the selected one are shown in red color.

- Start event logging by clicking Start Capture and stop it by clicking Stop Capture.
- The transactions can be saved in binary *.evt Event Log files by clicking **Save**. Saved Event Log files can be recalled by clicking **Open**.
- Clicking **Report** stores event logs as html reports to be shared and viewed with any web browser. The save dialog allows inclusion of detailed information about the DUT and the test in free-text *Report information*.

# **DP AUX Analyzer**

	Start Capture ata sources and filters: DisplayPort Output HPD UNDERSTAND USplayPort Input UNDERSTAND	■ S				er (DP Outp	ut port) ^{)/} DP AUX analyzer (DP Inp	ut port)	
	DisplayPort Output     HPD     AUX     OisplayPort Input					er (DP Outp	ut port) / DP AUX analyzer (DP Inp	ut port) 🔪	
	✓ · DisplayPort Input					Report	🔄 Open	_	
i			Line	Times	From	Туре	Details	Data	Message details:
			13	0.10	Source	Native	Reg RD 1 bytes from 0x00201		▲ Line #32 -
			14	0.11	Sink	Native	AUX_ACK - 1 bytes	00 00	111157311.79ms
	···· 📝 AUX		15	0.07	Source	Native	Req RD 1 bytes from 0x0000e		AUX_ACK - 16 bytes
	SDP		16	0.11	Sink	Native	AUX_ACK - 1 bytes Reg RD 12 bytes from 0x02200	00 80	
	MSA changes		17	0.07	Source	Native	AUX ACK - 12 bytes	00 14 1e	Extended Receiver
	VB-ID changes		19	0.16	Source	Native	Reg RD 1 bytes from 0x00021		Capability
	✓ USB-C DPRX		20	0.10	Sink	Native	AUX ACK - 1 bytes	00 01	DPCD_REV [RO]
			21	0.07	Source	Native	Reg WR 1 bytes to 0x02003	80 20 03	0x02200 := 0x14 DPCD V1.4
	📝 PD		22	0.12	Sink	Native	AUX ACK - 0 bytes	00	DPCD VI.4
	<ul> <li>USB-C DPTX</li> </ul>		23	0.06	Source	Native	Reg WR 1 bytes to 0x00111	80 01 11	Extended Receiver
	i 🔲 PD		24	0.12	Sink	Native	AUX ACK - 0 bytes	00	Capability
			25	0.06	Source	Native	Req RD 16 bytes from 0x00030	90 00 30	MAX LINK RATE [RO]
		<	26	0.11	Sink	Native	AUX_ACK - 16 bytes	00 2d 18	0x02201 := 0x1e
			27	0.20	Source	Native	Reg RD 1 bytes from 0x00000		MAX LINK RATE =
			28	0.11	Sink	Native	AUX_ACK - 1 bytes	00 14	8.1Gpbs
			29 30	0.07	Source	Native	Req RD 1 bytes from 0x0000e		
			30	0.11	Sink Source	Native Native	AUX_ACK - 1 bytes Reg RD 16 bytes from 0x02200	00 80	Extended Receiver
			32	0.07	Sink	Native	AUX ACK - 16 bytes	00 14 1e	Capability
			33	0.19	Source	Native	Reg RD 1 bytes from 0x00200		MAX_LANE_COUNT [RO]
			34	0.15	Sink	Native	AUX ACK - 1 bytes	00 41	0x02202 := 0xe4
			35	0.07	Source	Native	Reg RD 1 bytes from 0x00090		MAX_LANE_COUNT = 4 ENHANCED_FRAME_CAP
			36	0.11	Sink	Native	AUX ACK - 1 bytes	00 bf	= 1
			37	0.07	Source	Native	Reg RD 1 bytes from 0x00120	90 01 20	TPS3 SUPPORTED = 1
			38	0.11	Sink	Native	AUX_ACK - 1 bytes	00 3b	11-35_3011-01(12) = 1
			39	0.07	Source	Native	Req WR 1 bytes to 0x00120	80 01 20	POST LT ADJ REQ SUPPO
			40	0.12	Sink	Native	AUX_ACK - 0 bytes	00	RTED = 1
			41	0.06	Source	Native	Req RD 6 bytes from 0xf0000		
			42	0.12	Sink	Native	AUX_ACK - 6 bytes	00 00 00	Extended Receiver
			43	0.11	Source	Native	Reg WR 1 bytes to 0x00600	80 06 00	DETAILED CAP INFO AV
	Presets		<					>	DETAILED_CAP_INFO_AV

DP AUX Analyzer functionality is enabled in UCD-424 by default.

The AUX Analyzer tabs collect AUX Channel Transactions from the Event Log in the *Transaction list*. The user can parse the content of each transaction by clicking the corresponding *transaction line*. The parsed content is in the *Message Details* panel on the right.

Please refer to chapter *Customizing the Main Window* below for details on how to modify the content and look of the *Transaction list*.

### Lines

The data is organized in lines, each numbered starting from 1 and marked with a timestamp. There are four kinds of lines:

1. Information lines

Identified by the text "INFO" in their Type column, they provide some useful information like the time acquisition has started and stopped or the logical state of the inputs, etc.

2. Transaction lines

Identified by the text "Native" or "I2C" in their Type column, they report an AUX channel data transfer, either a data Request or a data Reply.

- **3.** Event lines Identified by the text "Event" in their Type column, they signal the state change in one or more of the monitored inputs.
- 4. Sideband Channel Messages The Isochronous Transport Service uses the sideband communications over sideband channel (AUX CH and HPD) for the management of topology/virtual channel connection/Main Link and performs Main Link symbol mapping.

### 5. Error lines

A line Type reading "Error" marks the detection of an illegal AUX channel data packet. An irregular start condition, an irregular stop condition or transfer of a number of bits which is not a multiple of 8 are all conditions that cause an error line.

**6.** Trace lines

Combines the data from several lines of a HDCP related message to one entry in *Message details* panel for easier readability.

### Columns

The data on each line is ordered in columns. Each column provides additional information about the data line, facilitating its viewing and interpretation:

#### Line

This column displays the line number, starting from 1, and cannot be hidden.

#### Timestamp

Each line is identified by its timestamp, marking the instant when an event or error was detected, or when a data transaction got started. The timestamp can be displayed as a time delay from the start of the acquisition (absolute) or from the previous line (relative). The timestamp can be displayed in milliseconds or in minutes, seconds and microseconds.

#### From

This column indicates the originator of the data line:

- "Source" and "Sink" for an AUX channel transaction, respectively a data Request and a data Reply.
- "Source Trace" and "Sink Trace" respectively for Sideband Message data Request and Reply.
- "Unknown" for signal state change events.

#### Туре

This column provides additional information about the type of the line:

- "Native" marks Native AUX channel Requests and Replies.
- "I2C" marks I2C AUX channel Requests and Replies.
- "Sideband Request" and "Sideband Reply" to mark the Sideband Channel messages
- **"Event**" is used for signal state change events.
- "**INFO**" is used with information lines.
- "Error" is used for illegal conditions detected on the AUX channel.

#### Details

This column contains an abbreviated description of the line content in textual form.

#### Data

The binary data exchanged during AUX channel transactions, in hexadecimal notation.

### Find

To locate an access to a DPCD location right-click on the list and select Find... or select Ctrl+F from keyboard. To Find again select F3.

Search				×	
Search for	h for Any access $\checkmark$ to addr. (Hex):				
	🗶 Cancel		9	Search	

### Message Details

The *Message details* panel is used to provide a detailed explanation of the line currently selected in the *Transaction list*. For AUX channel transaction lines, for each of the DPCD memory locations affected, the panel lists:

- All data bytes read or written.
- All DPCD memory locations affected.
- The name of the locations and of each of their bit fields.
- All bit field's numeric and binary values, together with their decoded value.
- The Replies outcome (AUX_ACK, AUX_NACK, I2C_DEFER, etc.).

### Customizing the Main Window

Format of the data shown in the *Transaction list* and the *Message details* panels can be altered in order to highlight the details of your interest.

#### **Selecting Data Columns**

The *Transaction list* can be customized by right-clicking over the list. The pop-up menu allows choosing which columns to display, the style of the timestamp and switch between absolute and relative timestamps. *Filters* limit the transactions shown in the list. Please see *Filtering* later in this document.



#### Selecting Font and Colors

Select **Tools > Options > AUX Analyzer options** tab. Click **Select new font** and choose the font and size used for displaying the *Transaction list* and the *Message details*.

Options			×	
Video, Audio and Misc options	AUX Analyzer options			
Font Selection	Font			×
Select new font Curren	Tahoma	Font style: Regular	Size: 10	OK
Transaction list color opt Show / change color settings	Tempus Sans ITC	A Regular Bold Oblique	10 1 11 12 14 16 18	Cancel
Normal item colors	Trebuchet MS	→ Bold Obl		
Color ex	car	Sample	AaBbYyZz	
Change text color		Script:		
Highlighted DPCD address	s r	Western	Ý	

### **Transaction List Color Options**

Select the colors for the font and background of various items.

ideo, Audio and Misc options AUX Analyzer options		
Font Selection		
Select new font Current font "Tahoma", size 10		
Transaction list color options		
Show / change color settings for:		
Normal item colors	~	
		l.
Normal item colors		
Selected item colors		l
Selected item colors Highlighted item colors		l
Selected item colors Highlighted item colors Sideband request message colors		
Selected item colors Highlighted item colors Sideband request message colors Sideband reply message colors		
Selected item colors Highlighted item colors Sideband request message colors Sideband reply message colors Signal state change message colors		
Selected item colors Highlighted item colors Sideband request message colors Sideband reply message colors		

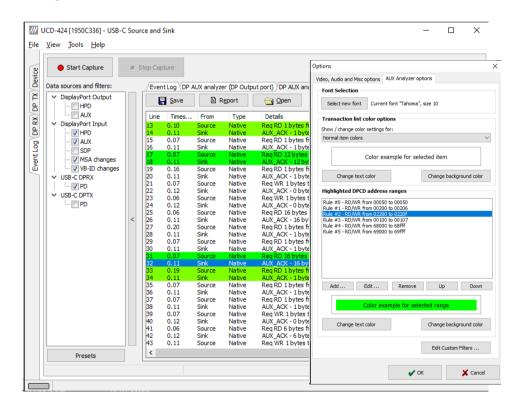
#### **Highlighted DPCD Address Ranges**

In order to improve the readability of the *Transaction list*, you can mark the AUX channel transactions where a certain DPCD register address or address range is highlighted with a color of choice.

Click **Add...**, select the access type, start DPCD address and end DPCD address of the range in Hex. Click **Accept**.

Select the range you just created from the **Highlighted DPCD addresses ranges** list and click the **Change test color** and **Change background color** buttons to select the colors desired.

You can create multiple simultaneous coloring rules to help you get a better view of the data captured.

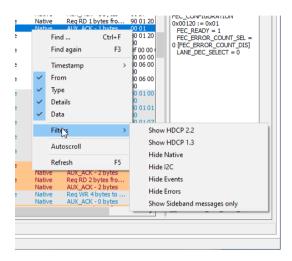


### Filtering

Transactions lines shown in the transaction list can be limited by *Filtering*. The shown lines can be selected by:

- The type of data line
- The origin of the message
- The DPCD address range

Right click > Filters drop down menu lists a set of pre-programmed filters.



### **Editing Filters**

From *Custom Filter* dialog (Tools > Options > Edit Custom Filters ...) allows for adding and modifying filters. The pre-programmed filters are listed in the dialog. Their structure can be copied as bases of your custom filters. It is advisable not to modify the pre-programmed filters directly but make copies of them.

Custo	m Filter					×
Stor	ed custor	m filter defin	itions			
	W HDCP 2					New definition
Hide	Native					Rename selected
	Events					Delete selected
	Errors v Sidebar	nd messages	only			Move Up
			,			Move Down
	r Rules Jest / Rep Rule	ly Pairing mo	ode Auto	Filter item by request if Range	reply received within 400 Comment	Dµs of request ∨
	Show	Native	Src/Sink	0x069000-0x069fff	Show HDCP 2.2. addre	ess range
Ad	ld	Edit	Remove	Up Down		
					🗶 Cancel	🖌 Accept

In the *Stored custom filter definitions* panel, lists currently defined Filters. On the right hand side buttons, you can define new Filters, rename or delete them. Their appearance in the *Filters* pull-down menu can also be altered.

In the *Filter Rules* panel lower in the dialog you can review and change the *Rules* in the selected *Filter*. Add... creates new rules, Edit... enables review and editing existing Filters and **Remove** deletes from the Filter definition.

When clicking Add... or Edit... *Edit Filter Rule* dialog opens. The dialog defines the action of the rule, events and event details.

/// Edit Filter Rule			-		×
Show $\checkmark$ Native	V From Source or Sink	✓ Range: 0x0	069000-0x069fff		
Filter by Data:					
					^
					~
Comment (Optional, max 120 chars):	Show HDCP 2.2. address ra	inge			
	🔗 Help	🗶 Canc	el	🖌 Accep	ot

Click **Help** to show "Help" text also attached to Appendix F of this document.

Note	Please note that Filters are a very powerful tool. They can however unintentionally hide valuable data from you. Please be careful when applying custom filters. A good practice is to start from an existing filter and gradually add new rules while testing their performance.
Note	Filtering and selecting the columns for display do not affect the actual data acquisition. All transactions and their full data are always captured.

# 10. EDID EDITOR

Collection 1	Details of ":/0/Version/Vendor Product	ID"	
<ul> <li>Blocks in collection</li> <li>Block 0 [VESA EDID]</li> </ul>	Key	Value	_
- Checksum	TD Manufacturer Name	UEG	
✓ · Version	ID Product Code	0x4036	
Extension flag	ID Froduct code ID Serial Number		
> Vendor & Product ID	ID Serial Number	0x3032344c	
> Basic Display Parameters and F			
> Display x,y Chromacity coordina	Manufacture or Model year	Manufacture Year and Week	
> Established timings I and II			
> Manufacturer's Timings	Week of manufacture	Week 52	
> Standard Timings	Year of manufacture	Year 2014	
<ul> <li>18-Byte data blocks</li> </ul>			
> Descriptor 1			
> Descriptor 2			
> · Descriptor 3			
> Descriptor 4			
<ul> <li>Block 1 [CEA 861]</li> </ul>			
Checksum			
✓ CEA Extensions Version			
···· Sink Underscans IT video ···· Basic audio			
···· YCbCr (4:4:4)			
>			

The EDID Editor main window is divided into three logical areas. The bottom part of the

window contains the command buttons, and the log view. The top-left portion shows the currently edited E-EDID blocks in a tree-form, and the top-right portion shows an edit control for the currently selected item, possibly a list of sub-keys and their names (The list is not shown for all values) and the HEX-view of the block collection.

### Command Buttons

Load: Load an EDID block collection file from disk. Save: Save the current block collection to a disk file. Show Hex: Show or Hide the HEX view. Show Log: Show or Hide the Log view.

### EDID Editor Features

The EDID Editor currently supports VESA E-EDID block versions 1.3 and 1.4. As the standard defines, the versions 1.0, 1.1 and 1.2 are supposed to be backward compatible, and therefore the VESA E-EDID decoder will also show their contents. However, in these cases it should be noted that the error checking is not compliant with restrictions given in these older versions of the standard. In addition to VESA E-EDID block, the CEA-861 versions 1, 2 and 3 EDID blocks are also fully supported as well as the VESA Block Map Extension blocks.

Practically unlimited number of extension blocks may exist in a single collection. The number of blocks is limited by VESA Specifications and possibly by available system resources. Most EDID blocks contain a structure that is very similar to a tree-structure. The EDID Editor decodes each block into a tree-view of the block. The tree-view then contains all values contained within the EDID block. The contents can then be easily browsed, using only a few mouse clicks. The EDID Editor has a support for automatic variables, such as the block checksum. When the user changes a value in an EDID block, the tool will update the checksum accordingly. The automatic variables appear as read only values for the user. A log print will be made when an automatic variable is updated by the editor.

**HEX View**: An optional HEX data display of all blocks in the collection. The view also shows the latest changes highlighted.

**LOG View**: An optional LOG view, which will contain log prints generated by the editor. Mostly it will list values that have been automatically updated due to edits.

### **Editing Tips**

Editing an EDID block is very straightforward, but there are some special cases where the user must know how to accomplish certain types of tasks.

- Enter key will apply text-edit values and combo-box selection.
- To apply new setting to *binary* values (ones that show a check-box), please click the **Set** button.
- When you see a **Quick Config** button appear below an editor, you can access a configuration menu that allows you to quickly select one of multiple pre-defined setup options.
- In CEA-861 blocks, you can add and remove 18-byte descriptors and CEA data blocks by setting the values "18-byte Descriptors in this block" and "CEA Data block count". Unfortunately re-arranging the descriptors and CEA data blocks is not supported yet, so you need to be careful when editing these.
- Enter hex values with prefix "0x" or "\$", no prefix means a decimal value.
- You can always enter HEX or DEC, even if the value is presented as HEX, and/or value range is given in HEX.
- Floating point values must be given with period "." as decimal separator, even if your localization setting defines decimal separator as comma (or other).
- Remember to click **Set** after changing a bit-value presented as a single check-box if you want the new value applied.

Note It is recommended that you back up the un-edited EDID contents to a file before editing and writing it to the card.

### Saving EDID Data

When you are done with editing you can either save the EDID contents to a file in the PC or bring it in the *HEX Editor*.

For saving the data to a file in your PC click Save.

For bringing the data to the HEX Editor close the EDID Editor window by clicking the **Window Close** button in the top right-hand corner of the window. You will be asked if you would like to copy and replace the EDID data in the HEX Editor. Click **Yes** to replace the data, click **No** to discard the modifications.

When you are back in the *HEX Editor*, the bytes that the *EDID Editor* changed are highlighted with **BLUE BACKGROUND**.

# APPENDIX A. PRODUCT SPECIFICATION

# UCD-424

Input (USB-C DP Rx)	USB-C & PD 3.0 compliant DRP port with DP 1.4a Alt Mode Receiver capability
Output (USB-C DP Tx)	USB-C & PD 3.0 compliant DRP port with DP 1.4a Alt Mode Transmitter capability
USB Pass Through	USB3.2 Gen2 data pass-through between test interfaces
Vbus Power	Up to 3A@9V input and output
Max video mode	7680 × 4320 p30 input and output 3840 × 2160 p120 input and output
Audio	LPCM, 2 – 8 channels, 44.1 to 192 kHz
Content Protection	HDCP 2.3, HDCP 1.3
DSC Capability	DSC DSC 1.2a sink with off-line decompression DSC DSC 1.2a source using pre-compressed content Support RGB / YCbCr up to 12 bits per component 24 slices, max with 7680 pixels
Additional features	FEC, LTTPR, DSC DP 1.4a LL CTS, DP DSC CTS HDCP 2.3 CTS
Computer interface	USB 3.0
Operating System	Windows 10, 8 and 7 macOS*, Linux* and Asterix* available Q2/20
Software	UCD Console GUI, TSI API with interface specific Test Sets
Power supply	AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +12 Vdc output)
Mechanical Size	310 × 190 × 61 mm
Weight	1.3 kg w/o power supply

*) Please contact Unigraf for detailed availability

# APPENDIX B. LICENSING

### UCD Console & TSI: USB-C DP Alt Mode Reference Sink (DP RX)

Тар	Function	Basic*	TSI Basic**	DSC Decoder	DP 1.4a LL CTS for testing Source DUT	HDCP 2.3 CTS for testing Source DUT	HDCP 2.3 CTS for testing Repeater DUT
USB-C							
	USB-C Data Role Status & Control	•	•				
	USB-C Power Role status & Control	•	•				
	USB-C Vbus / CC / Vconn voltage / current monitoring	•	•				
Video							
	Preview, Capture, Snap preview	•	•				
	Status	•	•			ſ	
Audio							
	Monitor, Capture and graphical preview	٠	•				
	Status	•	•				
Link							
	Link Status, Link Configuration	٠	•				
	Stream Status (video, audio)	•	•				
	HPD Status, HPD Assert / De-assert, HPD Long Pulse, HPD Short Pulse	•	•				
	MST Feature (up to 4 streams)	٠	•				
	FEC Feature	٠	•				
	DSC Decoder, DSC Configuration						
EDID							
	Read / Write, Save / Load	٠	•				
	EDID Editor	٠					
DPCD							
	Read/Write, Save/Load	٠	•				
	DPCD Decoder	٠					
HDCP							
	HDCP 1.3 and HDCP 2.3 Support	٠	•				
	Authentication status, Encryption status	•	•				
Event Log							
	Event Log	٠	•				
	DP AUX Analyzer	٠					
Source DUT Testing							
	Execute TSI Tests	٠	•				
	Execute DP LL, Audio and FEC CTS		1				
	Execute DSC CTS	1	1		1	1	
	HDCP 2.3 CTS for testing DP Source DUT	1	1		1		
	HDCP 2.3 CTS for testing DP Repeater DUT	1	l	1	1	1	

*) UCD-424 is delivered by default with UCD Console Pro for Type-C DP Sink, UCD Console Pro for Type-C DP Source and HDCP 2.3 support enabling license keys

**) UCD-424 is delivered by default with TSI SDK Advanced with HDCP 2.3 support key

	HDCP 2.3 CTS for testing DP Sink DUT							
		_						
	Execute DP LL, Audio and FEC CTS Execute DSC CTS			_				
		•	•					
Sink DUT Testing	Execute TSI Tests	-						
Sink DUT Testing	DP AUX Analyzer	•						
	Event Log	•	•					
Event Log	Eventled	-	_					
EventLea	IDCP 2.3 Support	•	•					
	Encryption status) HDCP 2.3 Support	_						
	Status: (Authentication status,	•	•					
	Encryption Enable / Disable, authenticate only, Encryption Enable / Disable)	•	•					
	HDCP 1.3 Support Control: (Enable / Disable, authenticate only,	•	•					
HDCP		_						
	DPCD Decoder	•						
	Read / Write, Save / Load	•	•					
DPCD								
	EDID Editor	•						
	Read / Write, Save / Load	•	•					
EDID								
	LTTPR Feature							
	DSC Encoder							
	FEC Feature	•	•					
	MST Feature (up to 4 streams)	•	•					
	Framing mode, Clock mode)	•	•					
	Link Configuration: (Lane count, Link Rate,							
	HPD Status: (Asserted / De-asserted)		•					
	Link Status	•	•					
Link		-	•					
	Play audio files	•	•					<u> </u>
Audio Generator		-	-					
	Adaptive Sync Feature	•	•					
	Fixed and custom Video Patterns		•					
Falleni Generaloi	Fixed and custom Video Timings	•	•					
Pattern Generator	current monitoring							
	USB-C Vbus / CC / Vconn voltage /	•	•					
	USB-C Power Role status & Control	•	•					
	USB-C Data Role Status & Control	•	•					
USB-C								
Tab	Function		*	er		TS DUT	TS DUT	TS er DUT
		Basic*	TSI Basic**	DSC Encoder	LTTPR	DP 1.4a LL CTS for testing Sink DUT	HDCP 2.3 CT for testing Sink [	HDCP 2.3 CT testing Repeate

*) UCD-424 is delivered by default with UCD Console Pro for Type-C DP Sink, UCD Console Pro for *Type-C DP Source* and *HDCP 2.3 support* enabling license keys **) UCD-424 is delivered by default with *TSI SDK Advanced with HDCP 2.3* support key

# APPENDIX C: PREDEFINED TIMINGS

## DisplayPort Sink and Source Capability (RGB) (4 lanes capability)

	1	1	•	5 (	, (			•		,,
Description	H active	V active	H total	V total	Frame rate	6	8	GB 4:4 10	:4 12	16
VESA 640 x 480 @ 60Hz	640	480	800	525	60	•	•	•	12	•
VESA 800 x 600 @ 60Hz	800	600	1056	628	60	•	•	•	•	•
VESA 848 x 480 @ 60Hz	848	480	1088	517	60	•	•	•	•	•
VESA 1024 x 768 @ 60Hz	1024	768	1344	806	60	•	•	•	•	•
CTA 1280 x 720 @ 60Hz	1280	720	1650	750	60	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1664	798	60	•	•	•	•	•
VESA 1280 x 960 @ 60Hz	1280	960	1800	1000	60	•	•	•	•	•
VESA 1280 x 800 @ 60Hz [RB1]	1280	800	1440	823	60	•	•	•	•	
VESA 1280 x 800 @ 60Hz	1280	800	1680	831	60	•	•	•	•	
VESA 1280 x 768 @ 60Hz	1280	768	1440	790	60	•	•	•	•	
VESA 1280 x 1024 @ 60Hz	1280	1024	1688	1066	60				•	
VESA 1260 x 768 @ 60Hz	1360	768	1792	795	60	•	•	•		•
VESA 1400 x 1050 @ 60Hz	1400	1050	1560	1080	60	•	•	•	•	•
VESA 1400 x 1050 @ 60Hz VESA 1600 x 1200 @ 60Hz [RB1]	1600	1200	1760	1235	60	•	•	•	•	•
				1255		•	•	•	•	•
VESA 1600 x 1200 @ 60Hz	1600	1200	2160		60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz	1680	1050	2240	1089	60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz [RB1]	1680	1050	1840	1080	60	•	•	•	•	•
VESA 1792 x 1344 @ 60Hz	1792	1344	2448	1394	60	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB1]	1920	1080	2080	1096	30	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB2]	1920	1080	2000	1096	30	•	•	•	•	•
CTA 1920 x 1080 @ 30Hz	1920	1080	2200	1125	30	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB1]	1920	1080	2080	1111	60	•	•	•	•	
VESA 1920 x 1080 @ 60Hz [RB2]	1920	1080	2000	1111	60	•	•	•	•	
CTA 1920 x 1080 @ 60Hz	1920	1080	2200	1125	60	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB1]	1920	1080	2080	1144	120	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB2]	1920	1080	2000	1144	120	•	•	•	•	•
CTA 1920 x 1080 @ 120Hz	1920	1080	2200	1125	120	•	•	•	•	•
VESA 1920 x 1440 @ 60Hz	1920	1440	2600	1500	60	•	•	•	•	•
VESA 2048 x 1536 @ 60Hz	2048	1536	2208	1580	60	•	•	•	•	•
VESA 2560 x 1440 @ 60Hz	2560	1440	2720	1481	60	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz	2560	1080	3424	1120	60	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz [RB1]	2560	1080	2720	1111	60	•	•	•	•	•
VESA 2560 x 1600 @ 60Hz	2560	1600	3504	1658	60	•	•	•	•	
VESA 2560 x 1600 @ 60Hz [RB1]	2560	1600	2720	1646	60	•	•	•	•	
Other 2880 x 1440 @ 60Hz	2880	1440	2976	1456	60	•	•	•	•	
VESA 4096 x 2160 @ 60Hz	4096	2160	4176	2222	60	•	•	•		
VESA 3840 x 2160 @ 30Hz [RB1]	3840	2160	4000	2191	30	•	•	•	•	
VESA 3840 x 2160 @ 30Hz [RB2]	3840	2160	3920	2191	30	•	•	•	•	•
CTA 3840 x 2160 @ 30Hz	3840	2160	4400	2250	30	•	•	•	•	•
CTA 3840 x 2160 @ 50Hz	3840	2160	5280	2250	50	•	•		-	
CTA 4096 x 2160 @ 50Hz	4096	2160	5280	2250	50	•	•			
VESA 3840 x 2160 @ 60Hz [RB1]	3840	2160	4000	2222	60	•	•	•		
VESA 3840 x 2160 @ 60Hz [RB2]	3840	2160	3920	2222	60	•	•	•		
CTA 3840 x 2160 @ 60Hz	3840	2160	4400	2250	60	•	•			
CTA 4096 x 2160 @ 60Hz	4096	2160	4400	2250	60	•	•			

Supported

Supported with HBR3

Description	Н	V	Н	V	Frame		R	GB 4:4	l:4	
Description	active	active	total	total	rate	6	8	10	12	16
VESA 3840 x 2160 @ 120Hz [RB1]	3840	2160	4000	2287	120					
VESA 3840 x 2160 @ 120Hz [RB2]	3840	2160	3920	2287	120					
CTA 3840 x 2160 @ 120Hz	3840	2160	4400	2250	120					
VESA 5120 x 2160 @ 30Hz [RB1]	5120	2160	5280	2191	30	•	•	•	•	•
VESA 5120 x 2160 @ 30Hz [RB2]	5120	2160	5200	2191	30	•	•	•	•	•
CTA 5120 x 2160 @ 30Hz	5120	2160	6000	2200	30	•	•	•	•	
VESA 5120 x 2160 @ 60Hz [RB1]	5120	2160	5280	2222	60	•	•			
VESA 5120 x 2160 @ 60Hz [RB2]	5120	2160	5200	2222	60	•	•			
CTA 5120 x 2160 @ 60Hz	5120	2160	5500	2250	60	•				
VESA 5120 x 2160 @ 120Hz [RB1]	5120	2160	5280	2287	120					
VESA 5120 x 2160 @ 120Hz [RB2]	5120	2160	5200	2287	120					
CTA 5120 x 2160 @ 120Hz	5120	2160	5500	2250	120					
Other 5120 x 2880 @ 60Hz	5120	2880	5280	2962	60	•				
VESA 7680 x 4320 @ 30Hz [RB1]	7680	4320	7840	4381	30					
VESA 7680 x 4320 @ 30Hz [RB2]	7680	4320	7760	4381	30					
CTA 7680 x 4320 @ 30Hz	7680	4320	9000	4400	30					
VESA 7680 x 4320 @ 60Hz [RB1]	7680	4320	7840	4443	60					
VESA 7680 x 4320 @ 60Hz [RB2]	7680	4320	7760	4443	60					
CTA 7680 x 4320 @ 60Hz	7680	4320	9000	4400	60					
VESA 7680 x 4320 @ 100Hz [RB1]	7680	4320	7840	4529	100					
VESA 7680 x 4320 @ 100Hz [RB2]	7680	4320	7760	4529	100					
CTA 7680 x 4320 @ 100Hz	7680	4320	10560	4500	100					

### DisplayPort Sink and Source Capability (RGB) (4 lanes capability) contd.

Supported

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Supported with HBR3

## DisplayPort Sink and Source Capability (YCbCr) (4 lanes capability)

Description	H	V	H	V	Frame		CbCr 4	· ·			CbCr 4	· ·	· /
·	active	active	total	total	rate	8	10	12	16	8	10	12	16
VESA 640 x 480 @ 60Hz	640	480	800	525	60	•	•	•	•	•	•	•	•
VESA 800 x 600 @ 60Hz	800	600	1056	628	60	•	•	•	•	•	•	•	•
VESA 848 x 480 @ 60Hz	848	480	1088	517	60	•	•	•	•	•	•	•	•
VESA 1024 x 768 @ 60Hz	1024	768	1344	806	60	•	•	•	•	•	•	•	•
CTA 1280 x 720 @ 60Hz	1280	720	1650	750	60	•	•	•	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1664	798	60	•	•	•	•	•	•	•	•
VESA 1280 x 960 @ 60Hz	1280	960	1800	1000	60	•	•	•	•	•	•	•	•
VESA 1280 x 800 @ 60Hz [RB1]	1280	800	1440	823	60	•	•	•	•	•	•	•	
VESA 1280 x 800 @ 60Hz	1280	800	1680	831	60	•	•	•	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1440	790	60	•	•	•	•	•	•	•	•
VESA 1280 x 1024 @ 60Hz	1280	1024	1688	1066	60	•	•	•	•	•	•	•	•
VESA 1360 x 768 @ 60Hz	1360	768	1792	795	60	•	•	•	•	•	•	•	•
VESA 1400 x 1050 @ 60Hz	1400	1050	1560	1080	60	•	•	•	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz [RB1]	1600	1200	1760	1235	60	•	•	•	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz	1600	1200	2160	1250	60	•	•	•	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz	1680	1050	2240	1089	60	•	•	•	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz [RB1]	1680	1050	1840	1080	60	•	•	•	•	•	•	•	•
VESA 1792 x 1344 @ 60Hz	1792	1344	2448	1394	60	•	•	•	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB1]	1920	1080	2080	1096	30	•	•	•	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB2]	1920	1080	2000	1096	30	•	•	•	•	•	•	•	•
CTA 1920 x 1080 @ 30Hz	1920	1080	2200	1125	30	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 60Hz [RB1]	1920	1080	2080	1111	60	•	•	•	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB2]	1920	1080	2000	1111	60	•	•	•	•	•	•	•	•
CTA 1920 x 1080 @ 60Hz	1920	1080	2200	1125	60	•	•	•	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB1]	1920	1080	2080	1144	120	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 120Hz [RB2]	1920	1080	2000	1144	120	•	•	•	•	•	•	•	•
CTA 1920 x 1080 @ 120Hz	1920	1080	2200	1125	120	•	•	•	•	•	•	•	•
VESA 1920 x 1440 @ 60Hz	1920	1440	2600	1500	60	•	•	•	•	•	•	•	
VESA 2048 x 1536 @ 60Hz	2048	1536	2208	1580	60	•	•	•	•	•	•	•	•
VESA 2560 x 1440 @ 60Hz	2560	1440	2720	1481	60	•	•	•	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz	2560	1080	3424	1120	60	•	•	•	•	•	•	•	
VESA 2560 x 1080 @ 60Hz [RB1]	2560	1080	2720	1111	60	•	•	•	•	•	•	•	•
VESA 2560 x 1600 @ 60Hz	2560	1600	3504	1658	60	•	•	•	•	•	•	•	
VESA 2560 x 1600 @ 60Hz [RB1]	2560	1600	2720	1646	60	•	•	•	•	•	•	•	
Other 2880 x 1440 @ 60Hz	2880	1440	2976	1456	60	•	•	•	•	•	•	•	
VESA 4096 x 2160 @ 60Hz	4096	2160	4176	2222	60	•	•	•		•	•	•	
VESA 3840 x 2160 @ 30Hz [RB1]	3840	2160	4000	2191	30	•	•	•	•	•	•	•	
VESA 3840 x 2160 @ 30Hz [RB2]	3840	2160	3920	2191	30	•	•	•	•	•	•	•	
CTA 3840 x 2160 @ 30Hz	3840	2160	4400	2250	30	•	•	•	•		•	•	
CTA 3840 x 2160 @ 50Hz	3840	2160	5280	2250	50	•	•	•			•	•	
CTA 4096 x 2160 @ 50Hz	4096	2160	5280	2250	50	•	•	•		•	•	•	
VESA 3840 x 2160 @ 60Hz [RB1]	3840	2160	4000	2222	60	•	•	•	•	•	•	•	
VESA 3840 x 2160 @ 60Hz [RB2]	3840	2160	3920	2222	60	•	•	•	•	•	•	•	-
CTA 3840 x 2160 @ 60Hz	3840	2160	4400	2250	60	•	•	•		•	•	•	
													-
CTA 4096 x 2160 @ 60Hz	4096	2160	4400	2250	60	•	•	•		•	•	•	

Supported

Supported with HBR3

DisplayPort Sink and Source	Capability	(YCbCr) (4 lanes	capability) contd.
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Description	Н	V	Н	V	Frame	YC	CbCr 4:	2:2 (bj	oc)	YC	CbCr 4	:2:0 (b	pc)
Description	active	active	total	total	rate	8	10	12	16	8	10	12	16
VESA 3840 x 2160 @ 120Hz [RB1]	3840	2160	4000	2287	120					•	•		
VESA 3840 x 2160 @ 120Hz [RB2]	3840	2160	3920	2287	120					•	•		
CTA 3840 x 2160 @ 120Hz	3840	2160	4400	2250	120					•			
VESA 5120 x 2160 @ 30Hz [RB1]	5120	2160	5280	2191	30	•	•	•	•	•	•	•	•
VESA 5120 x 2160 @ 30Hz [RB2]	5120	2160	5200	2191	30	•	•	•	•	•	•	•	•
CTA 5120 x 2160 @ 30Hz	5120	2160	6000	2200	30	•	•	•	•	•	•	•	•
VESA 5120 x 2160 @ 60Hz [RB1]	5120	2160	5280	2222	60	•	•	•		•	•	•	•
VESA 5120 x 2160 @ 60Hz [RB2]	5120	2160	5200	2222	60	•	•	•		•	•	•	•
CTA 5120 x 2160 @ 60Hz	5120	2160	5500	2250	60	•	•			•	•	•	
VESA 5120 x 2160 @ 120Hz [RB1]	5120	2160	5280	2287	120						-		
VESA 5120 x 2160 @ 120Hz [RB2]	5120	2160	5200	2287	120					•			
CTA 5120 x 2160 @ 120Hz	5120	2160	5500	2250	120								
Other 5120 x 2880 @ 60Hz	5120	2880	5280	2962	60	•				•	•	•	
VESA 7680 x 4320 @ 30Hz [RB1]	7680	4320	7840	4381	30	•				•	•		
VESA 7680 x 4320 @ 30Hz [RB2]	7680	4320	7760	4381	30	•				•	•		
CTA 7680 x 4320 @ 30Hz	7680	4320	9000	4400	30					•			
VESA 7680 x 4320 @ 60Hz [RB1]	7680	4320	7840	4443	60								
VESA 7680 x 4320 @ 60Hz [RB2]	7680	4320	7760	4443	60								
CTA 7680 x 4320 @ 60Hz	7680	4320	9000	4400	60								
VESA 7680 x 4320 @ 100Hz [RB1]	7680	4320	7840	4529	100								
VESA 7680 x 4320 @ 100Hz [RB2]	7680	4320	7760	4529	100								
CTA 7680 x 4320 @ 100Hz	7680	4320	10560	4500	100								

Supported

Supported with HBR3

## DisplayPort Sink and Source Capability (RGB) (2 lanes capability)

Description	H	V	H	V	Frame		1	GB 4:4		
	active	active	total	total	rate	6	8	10	12	16
VESA 640 x 480 @ 60Hz	640	480	800	525	60	•	•	•	•	•
VESA 800 x 600 @ 60Hz	800	600	1056	628	60	•	•	•	•	•
VESA 848 x 480 @ 60Hz	848	480	1088	517	60	•	•	•	•	•
VESA 1024 x 768 @ 60Hz	1024	768	1344	806	60	•	•	•	•	•
CTA 1280 x 720 @ 60Hz	1280	720	1650	750	60	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1664	798	60	•	•	•	•	•
VESA 1280 x 960 @ 60Hz	1280	960	1800	1000	60	•	•	•	•	•
VESA 1280 x 800 @ 60Hz [RB1]	1280	800	1440	823	60	•	•	•	•	•
VESA 1280 x 800 @ 60Hz	1280	800	1680	831	60	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1440	790	60	•	•	•	•	•
VESA 1280 x 1024 @ 60Hz	1280	1024	1688	1066	60	•	•	•	•	•
VESA 1360 x 768 @ 60Hz	1360	768	1792	795	60	•	•	•	•	•
VESA 1400 x 1050 @ 60Hz	1400	1050	1560	1080	60	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz [RB1]	1600	1200	1760	1235	60	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz	1600	1200	2160	1250	60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz	1680	1050	2240	1089	60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz [RB1]	1680	1050	1840	1080	60	•	•	•	•	•
VESA 1792 x 1344 @ 60Hz	1792	1344	2448	1394	60	•	•	•	•	
VESA 1920 x 1080 @ 30Hz [RB1]	1920	1080	2080	1096	30	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB2]	1920	1080	2000	1096	30	•	•	•	•	•
CTA 1920 x 1080 @ 30Hz	1920	1080	2200	1125	30	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB1]	1920	1080	2080	1111	60	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB2]	1920	1080	2000	1111	60	•	•	•	•	•
CTA 1920 x 1080 @ 60Hz	1920	1080	2200	1125	60	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB1]	1920	1080	2080	1144	120	•	•	٠		
VESA 1920 x 1080 @ 120Hz [RB2]	1920	1080	2000	1144	120	•	•	•		
CTA 1920 x 1080 @ 120Hz	1920	1080	2200	1125	120	•	•			
VESA 1920 x 1440 @ 60Hz	1920	1440	2600	1500	60	•	•	•	•	
VESA 2048 x 1536 @ 60Hz	2048	1536	2208	1580	60	•	•	•	•	
VESA 2560 x 1440 @ 60Hz	2560	1440	2720	1481	60	•	•	•		
VESA 2560 x 1080 @ 60Hz	2560	1080	3424	1120	60	•	•	•	•	
VESA 2560 x 1080 @ 60Hz [RB1]	2560	1080	2720	1111	60	•	•	•	•	
VESA 2560 x 1600 @ 60Hz	2560	1600	3504	1658	60	•	•			
VESA 2560 x 1600 @ 60Hz [RB1]	2560	1600	2720	1646	60	•	•	•		
Other 2880 x 1440 @ 60Hz	2880	1440	2976	1456	60	•	•	•		
VESA 4096 x 2160 @ 60Hz	4096	2160	4176	2222	60					
VESA 3840 x 2160 @ 30Hz [RB1]	3840	2160	4000	2191	30	•	•	•	-	
VESA 3840 x 2160 @ 30Hz [RB2]	3840	2160	3920	2191	30	•	•	•		
CTA 3840 x 2160 @ 30Hz	3840	2160	4400	2250	30	•	•	-		
CTA 3840 x 2160 @ 50Hz	3840	2160	5280	2250	50					
CTA 4096 x 2160 @ 50Hz	4096	2160	5280	2250	50	-				
VESA 3840 x 2160 @ 60Hz [RB1]	3840	2160	4000	2222	60					
VESA 3840 x 2160 @ 60Hz [RB2]	3840	2160	3920	2222	60					
CTA 3840 x 2160 @ 60Hz	3840	2160	4400	2250	60					
CTA 4096 x 2160 @ 60Hz	4096	2160	4400	2250	60	-				

Supported

Supported with HBR3

Description	Н	V	Н	V	Frame		R	GB 4:4	:4	
Description	active	active	total	total	rate	6	8	10	12	16
VESA 3840 x 2160 @ 120Hz [RB1]	3840	2160	4000	2287	120					
VESA 3840 x 2160 @ 120Hz [RB2]	3840	2160	3920	2287	120					
CTA 3840 x 2160 @ 120Hz	3840	2160	4400	2250	120					
VESA 5120 x 2160 @ 30Hz [RB1]	5120	2160	5280	2191	30	•	•			
VESA 5120 x 2160 @ 30Hz [RB2]	5120	2160	5200	2191	30	•	•			
CTA 5120 x 2160 @ 30Hz	5120	2160	6000	2200	30	•				
VESA 5120 x 2160 @ 60Hz [RB1]	5120	2160	5280	2222	60					
VESA 5120 x 2160 @ 60Hz [RB2]	5120	2160	5200	2222	60					
CTA 5120 x 2160 @ 60Hz	5120	2160	5500	2250	60					
VESA 5120 x 2160 @ 120Hz [RB1]	5120	2160	5280	2287	120					
VESA 5120 x 2160 @ 120Hz [RB2]	5120	2160	5200	2287	120					
CTA 5120 x 2160 @ 120Hz	5120	2160	5500	2250	120					
Other 5120 x 2880 @ 60Hz	5120	2880	5280	2962	60					
VESA 7680 x 4320 @ 30Hz [RB1]	7680	4320	7840	4381	30					
VESA 7680 x 4320 @ 30Hz [RB2]	7680	4320	7760	4381	30					
CTA 7680 x 4320 @ 30Hz	7680	4320	9000	4400	30					
VESA 7680 x 4320 @ 60Hz [RB1]	7680	4320	7840	4443	60					
VESA 7680 x 4320 @ 60Hz [RB2]	7680	4320	7760	4443	60					
CTA 7680 x 4320 @ 60Hz	7680	4320	9000	4400	60					
VESA 7680 x 4320 @ 100Hz [RB1]	7680	4320	7840	4529	100					
VESA 7680 x 4320 @ 100Hz [RB2]	7680	4320	7760	4529	100					
CTA 7680 x 4320 @ 100Hz	7680	4320	10560	4500	100					

Supported

Supported with HBR3

## DisplayPort Sink and Source Capability (YCbCr) (2 lanes capability)

Description	Н	V	Н	V	Frame		CbCr 4		. ,		CbCr 4	· ·	· /
·	active	active	total	total	rate	8	10	12	16	8	10	12	16
VESA 640 x 480 @ 60Hz	640	480	800	525	60	•	•	•	•	•	•	•	•
VESA 800 x 600 @ 60Hz	800	600	1056	628	60	•	•	•	•	•	•	•	•
VESA 848 x 480 @ 60Hz	848	480	1088	517	60	•	•	•	•	•	•	•	•
VESA 1024 x 768 @ 60Hz	1024	768	1344	806	60	•	•	•	•	•	•	•	•
CTA 1280 x 720 @ 60Hz	1280	720	1650	750	60	•	•	•	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1664	798	60	•	•	•	•	•	•	•	•
VESA 1280 x 960 @ 60Hz	1280	960	1800	1000	60	•	•	•	•	•	•	•	•
VESA 1280 x 800 @ 60Hz [RB1]	1280	800	1440	823	60	•	•	•	•	•	•	•	•
VESA 1280 x 800 @ 60Hz	1280	800	1680	831	60	•	•	•	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1440	790	60	•	•	•	•	•	•	•	•
VESA 1280 x 1024 @ 60Hz	1280	1024	1688	1066	60	•	•	•	•	•	•	•	•
VESA 1360 x 768 @ 60Hz	1360	768	1792	795	60	•	•	•	•	•	•	•	•
VESA 1400 x 1050 @ 60Hz	1400	1050	1560	1080	60	•	•	•	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz [RB1]	1600	1200	1760	1235	60	•	•	•	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz	1600	1200	2160	1250	60	•	•	•	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz	1680	1050	2240	1089	60	•	•	•	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz [RB1]	1680	1050	1840	1080	60	•	•	•	•	•	•	•	•
VESA 1792 x 1344 @ 60Hz	1792	1344	2448	1394	60	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 30Hz [RB1]	1920	1080	2080	1096	30	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 30Hz [RB2]	1920	1080	2000	1096	30	•	•	•	•	•	•	•	
CTA 1920 x 1080 @ 30Hz	1920	1080	2200	1125	30	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 60Hz [RB1]	1920	1080	2080	1111	60	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 60Hz [RB2]	1920	1080	2000	1111	60	•	•	•	•	•	•	•	
CTA 1920 x 1080 @ 60Hz	1920	1080	22000	1125	60	•	•	•	•	•	•	•	
VESA 1920 x 1080 @ 00112	1920	1080	2080	1144	120								-
• • •						•	•	•		•	•	•	
VESA 1920 x 1080 @ 120Hz [RB2]	1920	1080	2000	1144	120	•	•	•	•	•	•	•	•
CTA 1920 x 1080 @ 120Hz	1920	1080	2200	1125	120	•	•	•	•	•	•	•	•
VESA 1920 x 1440 @ 60Hz	1920	1440	2600	1500	60	•	•	•	•	•	•	•	•
VESA 2048 x 1536 @ 60Hz	2048	1536	2208	1580	60	•	•	•	•	•	•	•	•
VESA 2560 x 1440 @ 60Hz	2560	1440	2720	1481	60	•	•	•	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz	2560	1080	3424	1120	60	•	•	•	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz [RB1]	2560	1080	2720	1111	60	•	•	•	•	•	•	•	•
VESA 2560 x 1600 @ 60Hz	2560	1600	3504	1658	60	•	•	•		•	•	•	•
VESA 2560 x 1600 @ 60Hz [RB1]	2560	1600	2720	1646	60	•	•	•	•	•	•	•	•
Other 2880 x 1440 @ 60Hz	2880	1440	2976	1456	60	•	•	•	•	•	•	•	•
VESA 4096 x 2160 @ 60Hz	4096	2160	4176	2222	60					•	•		
VESA 3840 x 2160 @ 30Hz [RB1]	3840	2160	4000	2191	30	•	•	•	•	•	•	•	•
VESA 3840 x 2160 @ 30Hz [RB2]	3840	2160	3920	2191	30	•	•	•	•	•	•	•	•
CTA 3840 x 2160 @ 30Hz	3840	2160	4400	2250	30	•	•	•		•	•	•	•
CTA 3840 x 2160 @ 50Hz	3840	2160	5280	2250	50					•			
CTA 4096 x 2160 @ 50Hz	4096	2160	5280	2250	50					•			
VESA 3840 x 2160 @ 60Hz [RB1]	3840	2160	4000	2222	60	•				•	•		
VESA 3840 x 2160 @ 60Hz [RB2]	3840	2160	3920	2222	60	•				•	•		
CTA 3840 x 2160 @ 60Hz	3840	2160	4400	2250	60					•			
CTA 4096 x 2160 @ 60Hz	4096	2160	4400	2250	60					•			

Supported

Supported with HBR3

DisplayPort Sink and Source	Capability	(YCbCr) (2 lanes	capability) contd.
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Description	Н	V	Н	V	Frame	YC	CbCr 4	2:2 (bj	oc)	YC	CbCr 4	:2:0 (b	pc)
Description	active	active	total	total	rate	8	10	12	16	8	10	12	16
VESA 3840 x 2160 @ 120Hz [RB1]	3840	2160	4000	2287	120								
VESA 3840 x 2160 @ 120Hz [RB2]	3840	2160	3920	2287	120								
CTA 3840 x 2160 @ 120Hz	3840	2160	4400	2250	120								
VESA 5120 x 2160 @ 30Hz [RB1]	5120	2160	5280	2191	30	•	•	•		•	•	•	•
VESA 5120 x 2160 @ 30Hz [RB2]	5120	2160	5200	2191	30	•	•	•		•	•	•	•
CTA 5120 x 2160 @ 30Hz	5120	2160	6000	2200	30	•	•			•	•	•	
VESA 5120 x 2160 @ 60Hz [RB1]	5120	2160	5280	2222	60					•			
VESA 5120 x 2160 @ 60Hz [RB2]	5120	2160	5200	2222	60					•			
CTA 5120 x 2160 @ 60Hz	5120	2160	5500	2250	60								
VESA 5120 x 2160 @ 120Hz [RB1]	5120	2160	5280	2287	120								
VESA 5120 x 2160 @ 120Hz [RB2]	5120	2160	5200	2287	120								
CTA 5120 x 2160 @ 120Hz	5120	2160	5500	2250	120								
Other 5120 x 2880 @ 60Hz	5120	2880	5280	2962	60								
VESA 7680 x 4320 @ 30Hz [RB1]	7680	4320	7840	4381	30								
VESA 7680 x 4320 @ 30Hz [RB2]	7680	4320	7760	4381	30								
CTA 7680 x 4320 @ 30Hz	7680	4320	9000	4400	30								
VESA 7680 x 4320 @ 60Hz [RB1]	7680	4320	7840	4443	60								
VESA 7680 x 4320 @ 60Hz [RB2]	7680	4320	7760	4443	60								
CTA 7680 x 4320 @ 60Hz	7680	4320	9000	4400	60								
VESA 7680 x 4320 @ 100Hz [RB1]	7680	4320	7840	4529	100								
VESA 7680 x 4320 @ 100Hz [RB2]	7680	4320	7760	4529	100								
CTA 7680 x 4320 @ 100Hz	7680	4320	10560	4500	100								

Supported

d

Supported with HBR3

# APPENDIX D: PREDEFINED PATTERNS

Selection	Pattern	Description
Disabled	N/A	The links are activated but no video data transferred
Color Bar		100% intensity color bars of all primaries and mixed combinations.
Chessboard		8 by 8 chessboard with black (0%) and 100% intensity white
Solid Black		0% luminance
Solid White		100% white
Solid Red		100% red
Solid Green		100% green
Solid Blue		100% blue
White Vertical Stripes		Vertical stripes of black (0%) and white (100%). Parameters set the widths of the black and white stripes in pixels respectively. Default black / white = 20 / 20 pixels. Parameter range 0 to 5000.
Gradient Vertical Stripes		16 pixels high horizontal red green, blue and white stripes. Intensity is increased from 0 to 100% with steps defined by the given parameter (n). (step = $n*color_depth/256$ ). "n" range 0 to 5000 (default 120).
Color Ramp		Color Ramp test pattern defined by VESA DisplayPort Link Layer Compliance Test Specification.
Color Square		Color Square test pattern defined by VESA DisplayPort Link Layer Compliance Test Specification. Color mode can be selected between RGB, YCbCr 4:4:4, 4:2:2, 4:2:0 (ITU Rec 601 / 709)
White Square		100% intensity white square horizontally and vertically centered. Height and width defined by parameter as the percentage of height and width of the frame (default 30).
Motion Pattern		Horizontally moving color bar pattern. The pattern is shifted to left one pixel in each frame in a sequence. The length of the sequence is defined with parameter. Range 0 to 34 (default is 20)
Custom Image		Bitmap image uploaded by the user. Click on the <b>Custom</b> <b>Images</b> panel to browse. By default, Unigraf test image will be used.

More test patterns can be downloaded e.g. from www.icdm-sid.org/downloads/testpatterns.html.

# APPENDIX E: SINK, SOURCE AND REPEATER DUT TESTS

The tables below list the Unigraf TSI SDK Test Cases that you can run in *Sink DUT Testing / Source DUT Testing* tabs of UCD Console, their definition in *TSI Reference Manual* and the licensing needed.

Source DUT Testing		Default	DP 1.4a LL CTS*	DP DSC Decoder CTS*	DisplayID CTS*	Adaptive Sync CTS*	DP HDCP 2.3 CTS*
CRC based Video Test Set	CRC based single frame reference video test (TSI TEST VIDEO CRC SINGLE REF)	<b>~</b>					
	CRC based single frame stability test (TSI TEST CRC VIDEO STABILITY)	✓					
	CRC based sequence of frames reference video test (TSI TEST CRC VIDEO SEQUENCE)	✓					
	CRC based continuous sequence of frames reference video test (TSI_TEST_CRC_CONT_VIDEO_SEQUENCE)	✓					
Link Test Set	Link Training at All Supported Lane Counts and Link Rates (TSI_TEST_DP_SIMPLE_LINK)	~					
DP 1.4a Link Layer CTS	4.2.1.1 – 4.2.1.5, 4.2.2.1 – 4.2.2.10, 4.3.1.1 – 4.3.1.13, 4.3.2.1 – 4.3.2.5, 4.3.3.1, 4.4.1.1 – 4.4.1.3, 4.4.2, 4.4.3, 4.4.4.1 – 4.4.4.6, 4.5.1.1 – 4.5.1.2, 4.6.1.1 – 4.6.1.9		<b>~</b>				
DP 1.4a DSC CTS	4.6.1.1 - 4.6.1.9			<ul> <li>Image: A second s</li></ul>			
DisplayID / EDID CTS	4.7.1.1 – 4.7.1.4, 4.7.2.1 – 4.7.2.2, 4.7.3.1 – 4.7.3.3, 4.7.4.1				<ul> <li>Image: A start of the start of</li></ul>		
Adaptive Sync CTS	4.8.1.1 – 4.8.1.2, 4.8.2.1 – 4.8.2.2,					<ul> <li>Image: A second s</li></ul>	
HDCP 2.3 CTS 1A Test Set	HCDP2.3 CTS 1A-01 – HCDP2.3 CTS 1A-13						<ul> <li>Image: A start of the start of</li></ul>
HDCP 2.3 CTS 1B Test Set	HCDP2.3 CTS 1B-01 – HCDP2.3 CTS 1B-10						<b>√</b>

*) Separate licenses for testing Sink, Source, Branch (LL CTS, DSC, DisplayID, Adaptive Sync) DUT

Sink DUT Testing		Default	DP 1.4a LL CTS*	DP DSC Decoder CTS*	DisplayID CTS*	Adaptive Sync CTS*	DP HDCP 2.3 CTS*
DP 1.4a Link Layer CTS	$\begin{array}{l} 5.2.1.1-5.2.1.12, 5.2.2.1-5.2.2.9, 5.3.1.1-5.3.1.9,\\ 5.3.2.1-5.3.2.2, 5.4.1.1-5.4.1.4, 5.4.2, 5.4.3.1-5.4.3.2,\\ 5.4.4.1-5.4.4.6, 5.5.1.1-5.5.1.7, 5.6.1.1-5.6.1.26,\\ 5.6.2.1-5.6.2.14\end{array}$		*				
DP 1.4a DSC CTS	5.6.1.1. – 5.6.1.26, 5.6.2.1 – 5.6.2.14			<ul> <li>Image: A set of the set of the</li></ul>			
DisplayID / EDID CTS	5.7.1.1 - 5.7.1.5, 5.7.2.1 - 5.7.2.8, 5.7.3.1 - 5.7.3.5, 5.7.4.1 - 5.7.4.3, 5.7.4.5, 5.7.5.1 - 5.7.5.2, 5.7.6.1 - 5.7.6.5, 5.7.7.1 - 5.7.7.6, 5.7.7.1 - 5.7.7.6, 5.7.8.1 - 5.7.8.6, 5.7.9.1 - 5.7.9.3, 5.7.10.1 - 5.7.10.3, 5.7.11.1 - 5.7.11.5, 5.7.12.1 - 5.7.12.2				<b>~</b>		
Adaptive Sync CTS	5.8.1.1 – 5.8.1.3					<b>~</b>	
HDCP 2.3 CTS 2C Test Set	HCDP2.3 CTS 2C-01 – HCDP2.3 CTS 2C-06						<ul> <li>Image: A second s</li></ul>

Repeater DUT Testing		Default	DP HDCP 2.3 CTS*
HDCP 2.3 CTS 3A Test Set	HCDP2.3 CTS 3A-01 – HCDP2.3 CTS 3A-06		×
HDCP 2.3 CTS 3B Test Set	HCDP2.3 CTS 3B-01 – HCDP2.3 CTS 3B-07		✓
HDCP 2.3 CTS 3C Test Set	HCDP2.3 CTS 3C-01 – HCDP2.3 CTS 3C-25		✓

*) Separate licenses for testing Sink, Source, Branch (LL CTS, DSC, DisplayID, Adaptive Sync) DUT

# CRC Based Video Test Set – DP RX

### CRC Based Single Reference Frame Video Test

The test compares captured frames to a provided reference.

TE compares the video mode (Frame Width, Height, BPP and optionally Frame rate) to provided parameters and after that captures frames and compares the CRC (check sum) of their three color components to the provided reference until the number of bad frame limit provided is detected or the provided total number of frames is reached.

The test is judged FAIL if video mode does not match or the number of bad frames is exceeded.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

#### Parameters in use

- Test Timeout (default 100 000 ms)
- Total number of frames (default 2 000 ms)

- Number of bad frames allowed (default 2)
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Reference CRCs (R, G, B)

### CRC Based Single Frame Video Stability Test

The test verifies that the captured video is stable.

TE captures a frame and sets the CRC of its color components as reference. After that TE captures frames and compares their CRC (check sum) to the reference until the number of bad frame limit provided is detected or the provided total number of frames is reached.

The test is judged FAIL if the number of bad frames is exceeded.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

#### Parameters in use

- Test Timeout (default 100 000 ms)
- Total number of frames (default 2 000 ms)
- Number of bad frames allowed (default 2)

### **CRC Based Sequence of Reference Frames Test**

The verifies that a sequence of frames is captured in the right order.

TE compares the video mode (frame Width, Height, BPP and optionally Frame rate) to provided parameters. After that captures frames to find a frame with matching CRC (check sum) of their three color components to the first provided reference. After the first matching CRC is found it compares the CRC of the following frames until the Number of frames tested parameter is reached.

The test is judged FAIL if video mode does not match, the first frame in the list is not found or the CRC of the following frames do not match the provided list.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

#### Parameters in use

- Test Timeout (default 100 000 ms)
- Number of frames to be tested (default 20)
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Reference CRCs (R, G, B)

Note: Please note that in order for the TE to maintain the sequence, all CRCs in the reference frame list should be different.

### CRC Based Continuous Sequence of Reference Frames Test

The test verifies that a sequence of frames is captured in the right order many times repeatedly.

TE compares the video mode (frame Width, Height, BPP and optionally Frame rate and Color format) to provided parameters. After that captures frames to find a frame with matching CRC (check sum) of their three color components to the first provided reference. After the first matching CRC is found it compares the CRC of the following frames until the Number of frames tested parameter is reached. After that it resets the list and starts from the first CRC. The list is repeated until timeout or until the provided number of repetitions is reached.

The test is judged FAIL if video mode does not match, the first frame in the list is not found or the CRC of the following frames do not match the provided list.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

#### Parameters in use

- Test Timeout (default 100 000 ms)
- Number of frames to be tested (default 20)
- Number of iterations
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Expected color format
- Reference CRCs (R, G, B)

Note: Please note that in order for the TE to maintain the sequence, all CRCs in the reference frame list should be different.

# Link Test Set – DP RX

### Link Training at All Supported Lane Counts and Link Rates

Test requests link training on all supported lane counts and link rates. Each link training must be successfully completed in order to pass the test.

### Parameters in use

- Test Timeout (default 5 000 ms)
- Max lane count supported by DUT (default 4)
- Max lane rate supported by DUT as multiple of 0.27 Gbps. (valid settings 6, 10 and 20; default 20)
- Long HPD pulse duration (default 1 000 ms)
- Link training start timeout (default 5 000 ms)
- Delay between test cycles (default 3 000 ms)

# APPENDIX F: ADVANCED FILTERS

This the description of the advanced methods for filtering transactions in *DP AUX analyzer* in *Event Log*. The following help text can be seen as well by clicking the Help button of the *Edit Filter Rule* dialog.

Note Please note that Filters are a very powerful tool. They can however unintentionally hide valuable data from you. Please be careful when applying custom filters. A good practice is to start from an existing filter and gradually add new rules while testing their performance.

Note Filtering and selecting the columns for display do not affect the actual data acquisition. All transactions and their full data are always captured.

#### Data pattern expressions

A data-pattern expression is a string that describes how to determine if a data-block should be considered as "matched" or "unmatched". The syntax used with data-pattern expressions in Aux Channel Analyzer is described below

The data-block must be covered completely by the data-pattern expression. If the data block is shorter, or longer than the expression, then the data block is determined as "not matched". The '*' wildcard can be used to allow data blocks of any size to match.

Whitespaces and new-lines are ignored and are allowed anywhere; White spaces and new-lines can be used strategically to make the expression more readable.

For example: "*!(10)??(10)" is the same as "* ! (10) ? ? (10)"

#### Comment blocks:

Comments must be written enclosed in curly-braces '{' and '}'.

#### Wildcards

Wildcards used are '*' and '?'

? = Match any single data byte only.

* = Match any number of any data bytes. (including the possibility of matching NO data bytes)

For data matching, the byte value must be enclosed in braces '(' and ')'. Use prefixes '\$' to indicate HEX value, '%' to indicate BIN. No prefix indicates DEC.

#### Examples:

* (\$10) (\$00) : Matches any data pattern that has the bytes \$10, \$00 at end of data.

? (\$10) (\$00) : Matches 3-byte data pattern that has \$10 as second byte and \$00 as third byte.

* (\$10) * (\$00) : Matches any data pattern that has \$10 and ending to a \$00 byte.

* (\$10) * (\$00) *: Matches any data pattern that has \$10 and \$00 after it.

(\$10) ? * (\$20) * : Matches any data pattern that has \$10 as first byte, followed by \$20 with at least one other byte in between. (i.e. will not match \$10, \$20)

#### Use '!' to invert the match:

!(\$00) = Match any data byte that isn't \$00.

#### Use '?' within HEX or BIN value to ignore that bit in comparison:

(\$??) = ? = Any data Byte.

(\$?0) = Any data byte with bits 0-3 cleared.

(%1??????) = Any data byte with bit 7 set.

(%0?????1) = Any data byte with bit 7 cleared and bit 0 set.

The '!' inversion can still be used:

!(%?????00) = Matches any data byte ending to %10, %11, %01 but not %00.

To match a single data byte with more than one value, separate the values with comma ',':

(0, 1, 100, 200, 254) : Matches a data byte whose value is 0, 1, 100, 200 or 254.

Invert the value group match with '!'. Value wildcard '?' is also allowed.

#### Example:

!(1, 2, 3): Match any data byte other than 1, 2 or 3.

!(\$?f, \$f?): Don't match data bytes with bits 0-3 set to 1, or data bytes that have bits 7-4 set.

# APPENDIX G: FIRMWARE RECOVERY PROCEDURE WITH QUARTUS PRIME

# FW Update Tool

The chapter below describes a procedure for updating UCD-424 Firmware in a case when e.g. the normal FW Update procedure failed because a critical error.

- Download the latest UCD-300/400 SW Bundle version from Unigraf website <u>https://www.unigraf.fi/downloads/</u> and install it. Please do not launch UCD Console yet.
- *Recovery.zip* file will be by default installed in <u>C:\Program Files (x86)\Unigraf\TSI\UCD-400\Recovery</u>.
   Perform the *Recovery Procedure* according to the instructions on the following pages.
- ▶ Without removing power from the UCD-424 device perform FW update procedure as described in section 4 FIRMWARE UPDATE PROCEDURE earlier in this manual.

**Note** The FW patch loaded in the UCD device during Recovery procedure is stored in a temporary memory. When power is removed from UCD device, the content of the temporary memory will be erased. Therefore, please do not power down the UCD device after performing the *Recovery* before instructed in the end of the FW Update procedure.

If power will accidentally be removed before the FW Update procedure, Recovery procedure needs to be re-initiated.

# **Recovery Procedure**

The Recovery patch is programmed to UCD Device with a separate tool called **Quartus Prime (includes Nios II EDS)**. The tool can be downloaded from **Intel® FPGA** website:

https://fpgasoftware.intel.com/16.1/?edition=lite&platform=windows

On the download page, please **Select release 16.1.** Please download **Quartus Prime** (includes Nios II EDS).

ease date: November, 2016 est Release: v19.1	Intel' Quartus' Prime Design Software
ect release: 16.1 • Please select release 1	.6.1
erating System ݬ 🛛 👫 Windows 🖲 Å Linux	
A newer version of the Quartus Prime Design Software is a Quartus Prime Design Software. This version does not include and security updates. For critical support requests, please cor	e the latest open source components that have function
You may be exposed to a vulnerability issue if you have in: rom v11.0 to v18.0 to a location with space(s) in the path. See	· · · · · · · · · · · · · · · · · · ·
The Quartus Prime Lite software version 16.1 supports the MAX II, MAX V, and MAX 10 FPGA. <a href="https://www.markage.com"><u>More</u></a>	e following device families: Arria II, Cyclone IV, Cyclone V
	0
Combined Files Individual Files Additional Softw	vare Updates
Download and install instructions: <u>More</u>	rare Updates
	rare Updates
Download and install instructions: <u>More</u> Read Intel FPGA Software v16.1 Installation FAQ	rare Updates
Download and install instructions: <u>More</u> Read Intel FPGA Software v16.1 Installation FAQ	
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Note: Registering is needed for the download.

Please download and install the tool in the PC.

### Connect to the UCD-424 Unit

- Power on the UCD-424.
- Connect UCD-424 with a USB cable to the PC through Programmer connector. (Pls refer to page 8 of this document)

### Programming the FW

Please locate the *Recovery.zip* file. It is by default installed in <u>C:\Program Files (x86)\Unigraf\TSI\UCD-400\Recovery</u>. Extract the content of the zip file in a folder in your PC, e.g., c:\Temp

Run Nios II 16.1 Command Shell application as Administrator

Note:	Nios II 16.1 Command Shell application needs to be run as Administrator (Right click with mouse and select <b>Run as Administrator</b> )
Hint:	Right click on the top edge of <i>Command Shell</i> and select <b>Edit &gt; Paste</b> to paste the commands below
►	Select the folder location where the content of the <i>Recovery.zip</i> file was extracted. For example (C:/Temp) cd /cygdrive/c/Temp
►	Run the loader.
	source recovery.sh
	This instruction will load a temporary patch to the FW of the UCD Device to enable normal FW Update procedure
►	Once the upload has completed, please close the commend shell.
•	Launch UCD Console and initiate FW Update by selecting Tools > Firmware update. Please follow the instructions given in section 4 FIRMWARE UPDATE PROCEDURE earlier in this manual.
Note	The FW patch loaded in the UCD device during Recovery procedure is stored in a temporary memory. When power is removed from UCD device, the content of the temporary memory will be erased. Therefore, <b>please do not power down</b> the UCD device after performing the Recovery before instructed in the end of the FW Update procedure.
	If power will accidentally be removed before the FW Update procedure, Recovery procedure needs to be re-initiated.
►	Once FW update procedure has completed, cycle power on the UCD Device (switch off power > wait for 10 seconds > turn on power).
Note	Please cycle the power on the UCD-424 unit to enable the FW update (switch off power > wait for 10 seconds > turn on power).
	After Recovery procedure has been completed, you can delete the files stored in e.g., C:/Temp.