

USB Power Delivery

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Agenda

- Introduction
- Charging
- USB4™
- Compliance

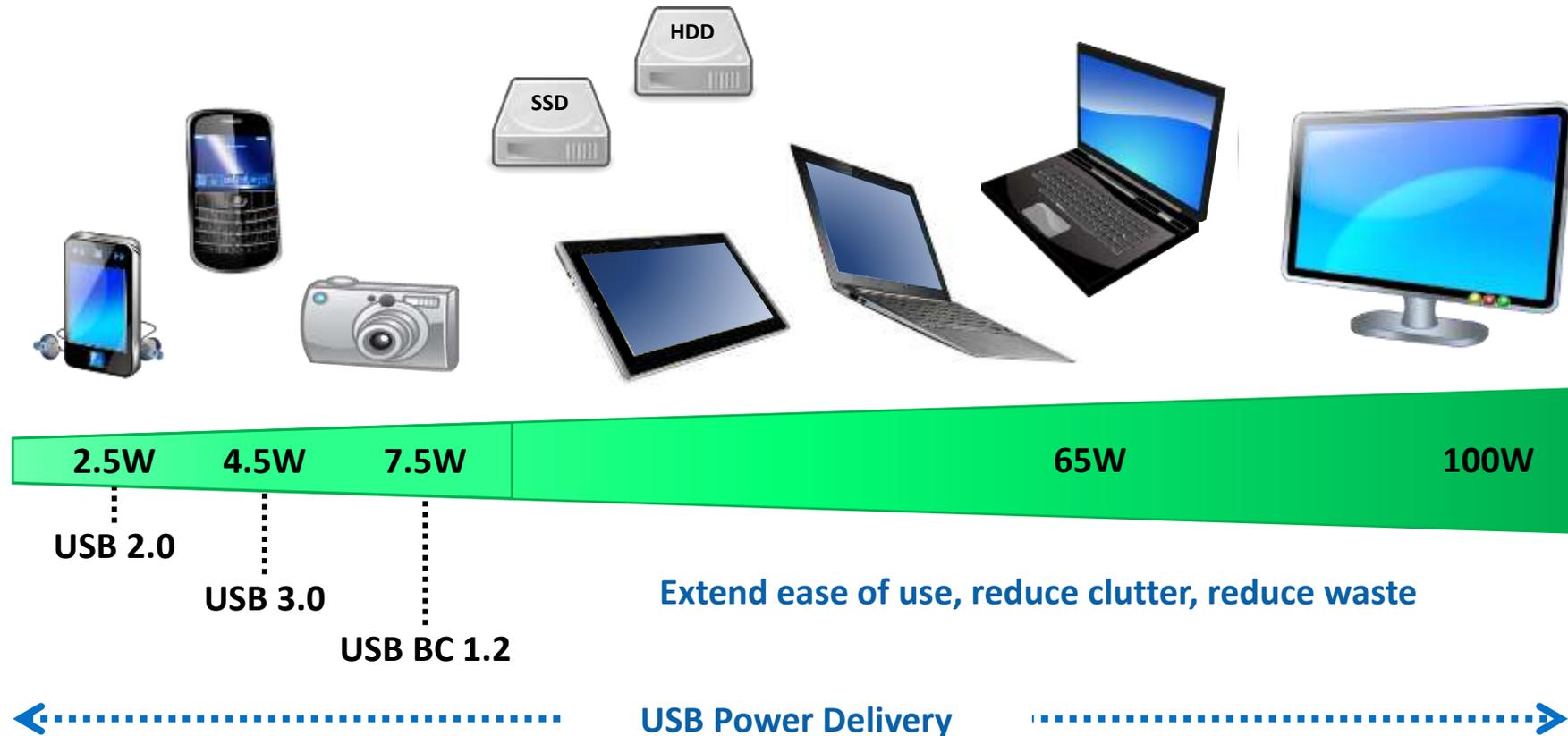
Agenda

- **Introduction**
- Charging
- USB4™
- Compliance

Introduction

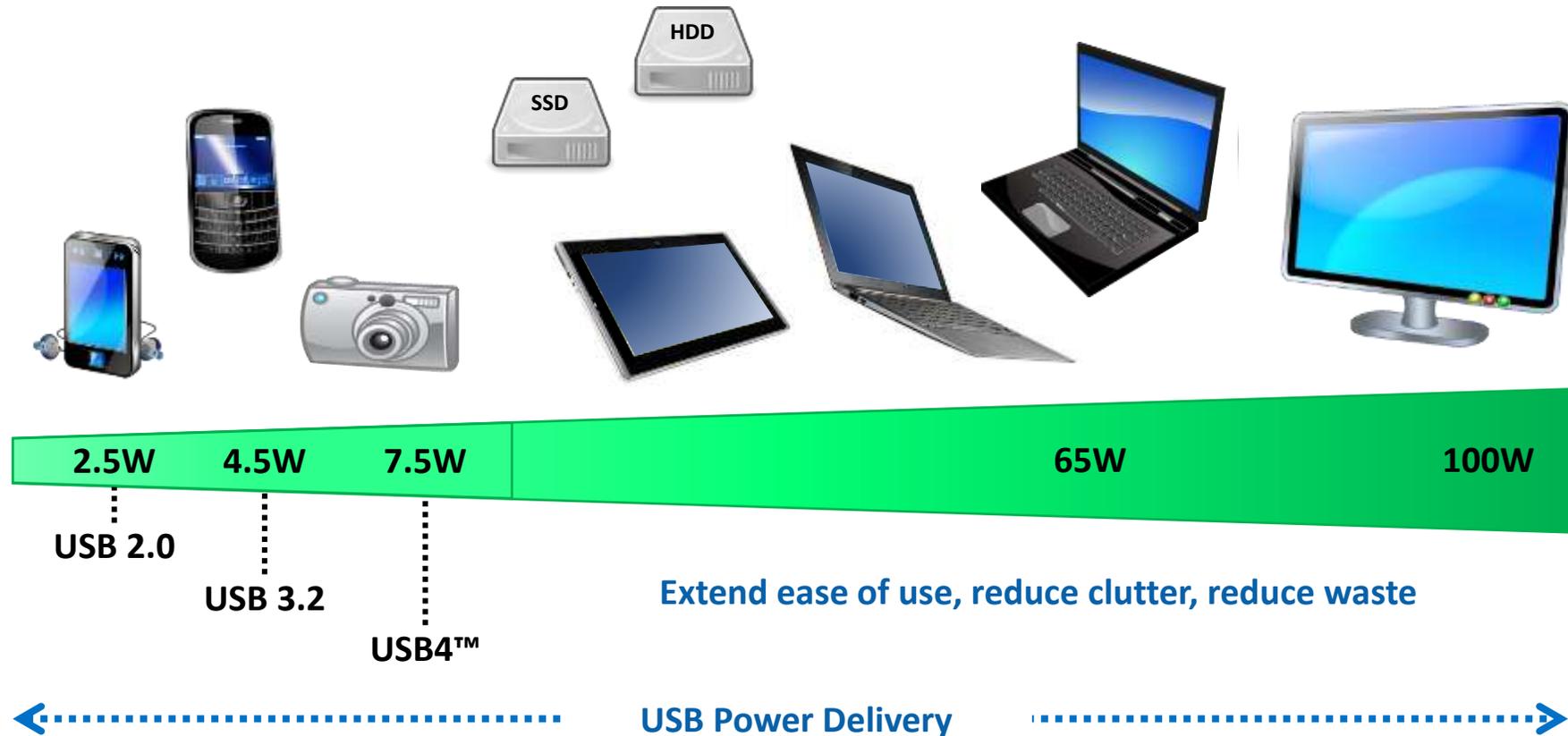
- **What is Power Delivery?**
- New in the latest specification

Our vision...



- Power increased to ~100W
- Concept of universal charging being extended by IEC 63002

The realization ...



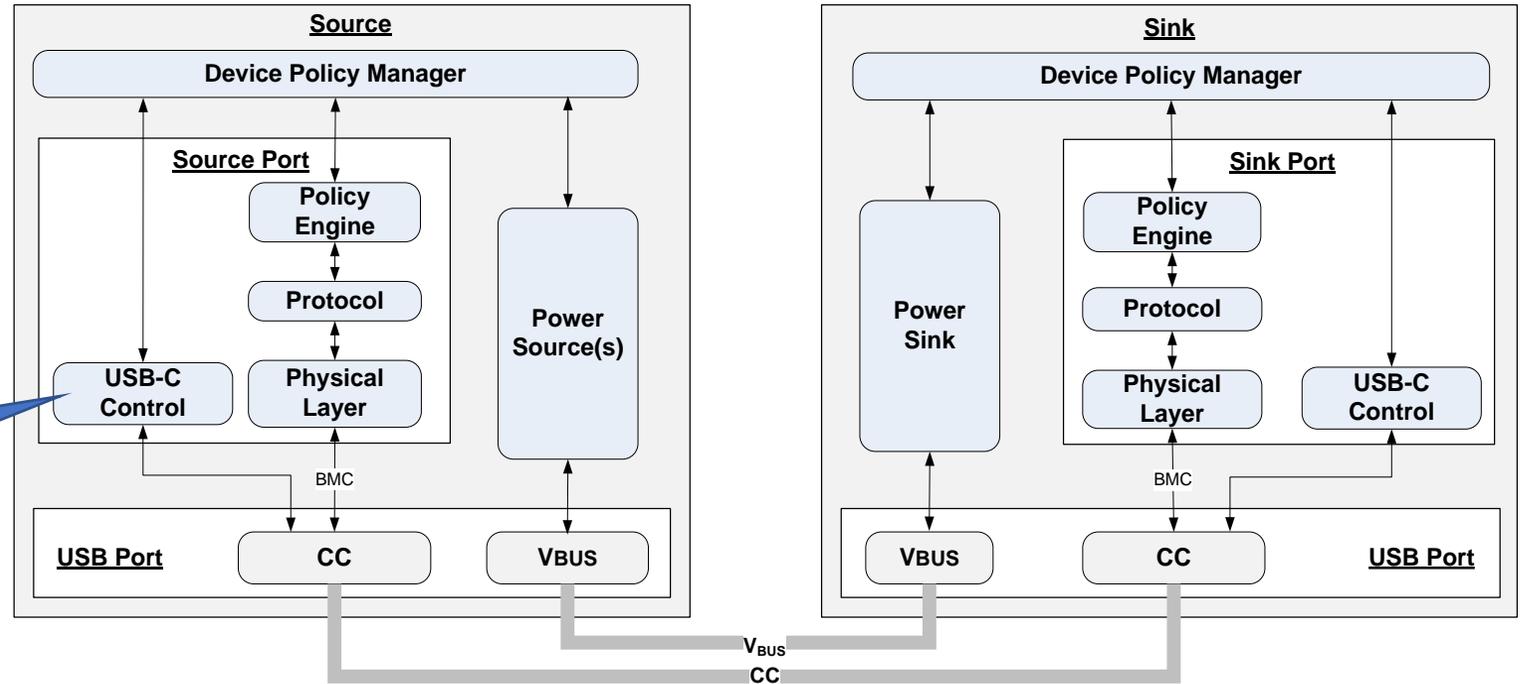
- Power increased to ~100W
- Concept of universal charging extended by IEC 63002
- PD is extensible
 - Added PPS for faster charging
 - PD as a sideband (Discovery, Alternate Modes, USB4 etc.)

Terminology

- DFP/UFP
 - Defines the Port's position in the USB topology
 - DFP is equivalent to A-Port/Host, UFP is equivalent to B-Port/Device
 - Does not imply USB Communication Capability
- Source/Sink
 - Defines the power role the port is currently operating in
- DRP (Dual-role Power)
 - Port can operate as either a Source or a Sink
- DRD (Dual-role Data)
 - Port can operate as either a DFP or a UFP
- SOP*
 - Start of packet (SOP/SOP'/SOP'')
- PDP Rating
 - Power Delivery Power Rating – akin to the wattage rating of a light bulb

USB PD System Overview

USB Type-C® Specification



- USB Type-C Port Control
 - USB Type-C state operation (attach/detach)
- Physical Layer
 - Port to Port over CC wire
 - Collision Avoidance
- Protocol Layer
 - Handles retries, message construction and chunking

- Power Source/Sink
 - Controls power transitions
- Device Policy
 - Policy Engine
 - Drives the Atomic Message Sequences
 - Device Policy Manager
 - Handles PD across multiple ports
 - Makes decisions on how to allocate power
 - Talks to Power Source/Sink and Cable Detection

How it works

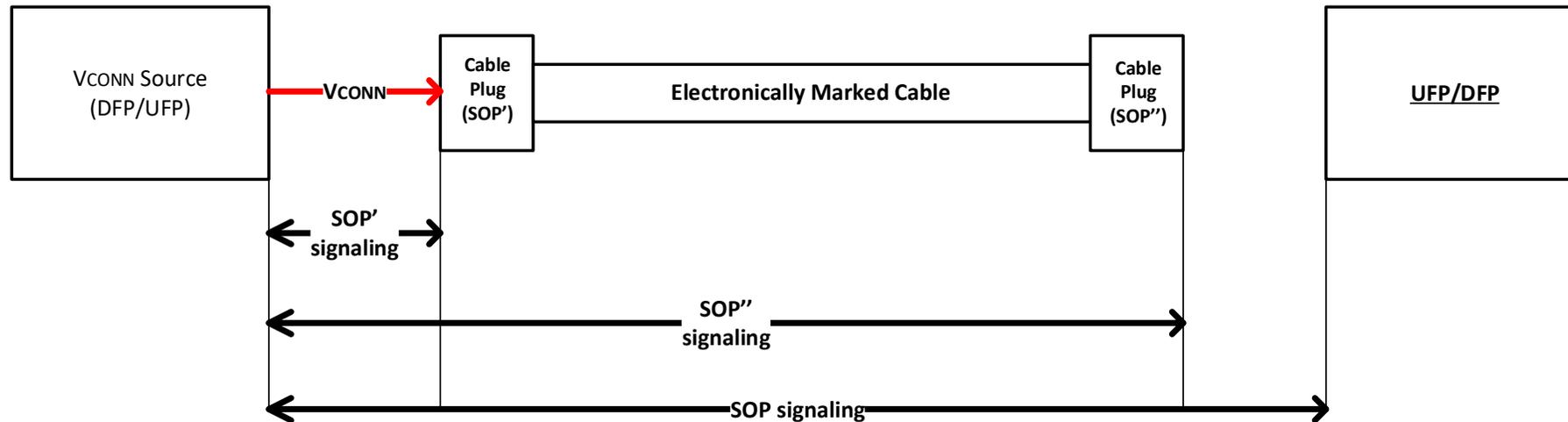
- Negotiating power is simple and robust
 - Source sends its capabilities
 - Sink makes a Request
 - Source Accepts and send PS_Ready
- What happens when the Sink needs more power?
 - Sink can indicate that it needs more power (Capability Mismatch)
 - Source can read Sink's capabilities to determine what it needs to function
- Extended capabilities used to exchange additional information between Source and Sink
- Status provides real-time operational information

USB Type-C[®] Alternate Modes

- Alternate modes reconfigure the connector
 - Repurpose pins to support another bus
 - Change the mode of operation of a bus
 - Enable sideband signals
- Alternate modes may reconfigure the cable
 - Change signal conditioning type or direction
- *Note: Accessory Mode is not the same*

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	VCONN			SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Multi-drop used to access cable



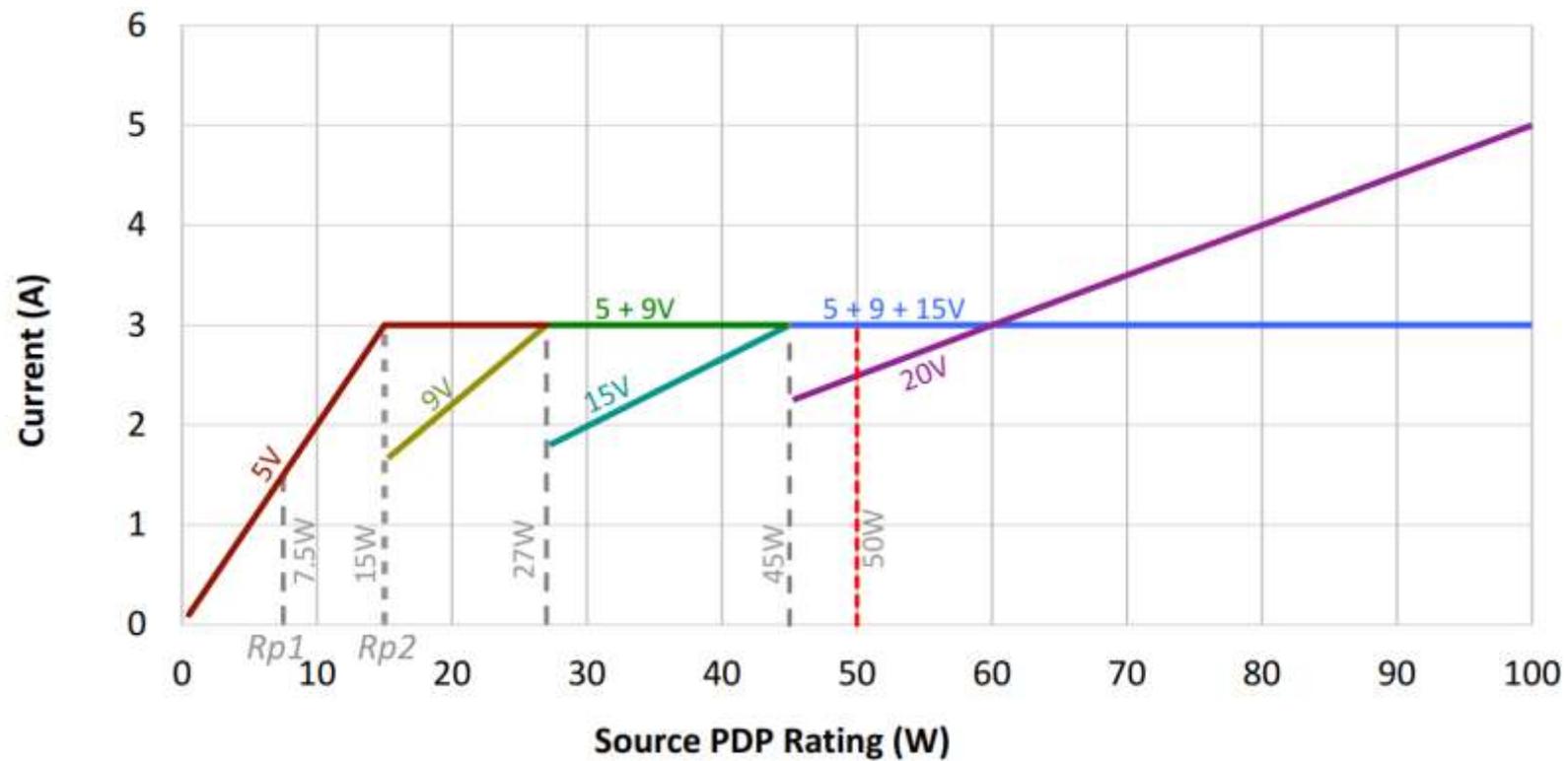
- Multi-drop
 - Packet structure unchanged
 - Start of packet is message 'address' (SOP'/SOP'')
 - Limited access to the new 'addresses'
 - Electronically marked cables respond to SOP'
- Only the VCONN Source can reliably talk to the cable
 - Source of VCONN controlled via with VCONN_Swap
- Single initiator of multi-drop message sequences
 - Cable Plug not allowed to initiate messages
 - Source allowed to initiate communication SOP' prior to an explicit contract
 - DFP can initiate communication SOP'/SOP'' within an explicit contract

Discover Identity

- General information
 - Type of product
 - Modal Operation
 - XID
 - VID
 - PID
 - bcdDevice
- Used to get information about the cable (e-marker) e.g.
 - Speed
 - Current carrying capability
- Now additional information for Ports

PDP

- PDP defined to enable good interoperability between Sources and Sinks
 - Capability is incremental; higher rated Sources also look like lower rated Sources
- Manufacturer declared value placed on Source packaging:
 - Defines voltages for PDOs and APDOs (fixed supply/PPS)
 - Used to calculate current values for each voltage PDO/APDO
 - Fixed rounded to nearest 20 mA
 - PPS rounded to nearest 50 mA
- Sinks designed to operate with a given PDP rating:
 - Function correctly with a Source of the PDP rating or higher
 - May have a reduced functionality with lower PDP rating



Fixed Supplies

Table 10-3 Fixed Supply PDO – Source 5V

Bit(s)	Description								
B31...30	Fixed supply								
B29	Dual-Role Power								
B28	USB Suspend Supported								
B27	Unconstrained Power								
B26	USB Communications Capable								
B25	Dual-Role Data								
B24...22	Reserved – Shall be set to zero.								
B21...20	Peak Current								
B19...10	5V								
B9...0	Current based on PDP <table border="1"> <thead> <tr> <th>PDP Rating (x)</th> <th>Current (A)</th> </tr> </thead> <tbody> <tr> <td>$0.5 \leq x \leq 15$</td> <td>$x \div 5$</td> </tr> <tr> <td>$15 < x \leq 25$</td> <td>$3 \leq A \leq x \div 5$</td> </tr> <tr> <td>$25 < x \leq 100$</td> <td>$3 \leq A \leq 5$</td> </tr> </tbody> </table>	PDP Rating (x)	Current (A)	$0.5 \leq x \leq 15$	$x \div 5$	$15 < x \leq 25$	$3 \leq A \leq x \div 5$	$25 < x \leq 100$	$3 \leq A \leq 5$
PDP Rating (x)	Current (A)								
$0.5 \leq x \leq 15$	$x \div 5$								
$15 < x \leq 25$	$3 \leq A \leq x \div 5$								
$25 < x \leq 100$	$3 \leq A \leq 5$								

Table 10-4 Fixed Supply PDO – Source 9V

Bit(s)	Description										
B31...30	Fixed Supply										
B29...22	Reserved – Shall be set to zero.										
B21...20	Peak Current										
B19...10	9V										
B9...0	Current based on PDP <table border="1"> <thead> <tr> <th>PDP Rating (x)</th> <th>Current (A)</th> </tr> </thead> <tbody> <tr> <td>$0.5 \leq x \leq 15$</td> <td>PDO not required</td> </tr> <tr> <td>$15 < x \leq 27$</td> <td>$x \div 9$</td> </tr> <tr> <td>$27 < x \leq 45$</td> <td>$3 \leq A \leq x \div 9$</td> </tr> <tr> <td>$45 < x \leq 100$</td> <td>$3 \leq A \leq 5$</td> </tr> </tbody> </table>	PDP Rating (x)	Current (A)	$0.5 \leq x \leq 15$	PDO not required	$15 < x \leq 27$	$x \div 9$	$27 < x \leq 45$	$3 \leq A \leq x \div 9$	$45 < x \leq 100$	$3 \leq A \leq 5$
PDP Rating (x)	Current (A)										
$0.5 \leq x \leq 15$	PDO not required										
$15 < x \leq 27$	$x \div 9$										
$27 < x \leq 45$	$3 \leq A \leq x \div 9$										
$45 < x \leq 100$	$3 \leq A \leq 5$										

- Fixed voltage outputs:
 - 5 V, 9 V, 15 V and 20 V depending on PDP
 - Optional voltages may additionally be supported
- Output current capability depends on PDP and cable rating
 - PDO Current = PDP/Voltage rounded to the nearest 10 mA

Programmable Power Supply (PPS)

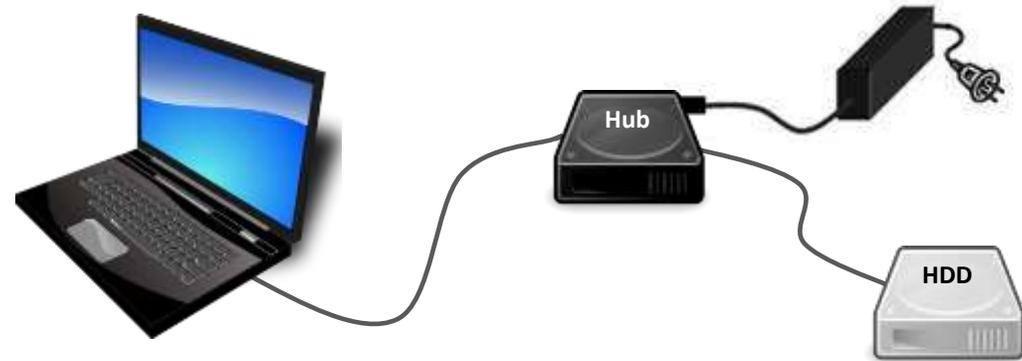
	Fixed Nominal Voltage			
	5V Prog	9V Prog	15V Prog	20V Prog
Maximum Voltage	5.9V	11V	16V	21V
Minimum Voltage	3.3V	3.3V	3.3V	3.3V

- Output voltage ranges:
 - 5V Prog, 9V Prog, 15V Prog and 20V Prog depending on PDP
 - Optional voltage ranges may additionally be supported
- Output current capability depends on PDP and cable rating
 - APDO Current = PDP/Prog Voltage rounded to the nearest 50 mA

- Sink Directed Charging
 - Sink periodically (at least every 10 seconds) requests Voltage/Current
 - Source operates in constant voltage mode or current limit mode depending the on load
 - Source provides status (operational mode, voltage and current)
 - Source returns to its safe state when communications with the Sink are lost
- Safety first!
 - Over Current/Over Temperature protection required
 - Periodic communications with Sink required
 - Alerts for OC/OT events

Fast Role Swap

- Initial Source (Hub) has power removed
 - Maintains power to downstream peripherals
 - Stops sourcing power upstream
 - Needs new power source urgently!
 - Signals Fast Swap on CC line
- Initial Sink (Laptop) has 5 V Source ready to be applied quickly
 - Detects Fast Swap
 - Waits for supply to drop to 5 V
 - Starts Sourcing 5 V
- In parallel Port Partners start the role swap process
 - Ensures that Source and Sink roles are aligned



Introduction

- What is Power Delivery?
- **New in the latest specification**

New in the latest specification

- Moving from emphasis on USB Power Delivery for controlling power to also use as the USB4™ discovery and entry
- New features/updates:
 - Charging
 - Fixed supply
 - PPS
 - Multi-port chargers
 - USB4
 - Cables
 - Fast/Power Role Swap
 - Misc.

Charging – Fixed Supply

- No Load transition overshoot settling time for PDO ($t_{SrcTransient}$) relaxed for loads < 60 mA
- 60 mA is the minimum load that will result in a 5 ms settling time based on $3000 \mu\text{F} * (0.1 \text{ V}) / 5 \text{ ms} = 60 \text{ mA}$
- $t_{SrcTransient}$
 - 5 ms max for loads ≥ 60 mA
 - 150 ms max < 60 mA

Charging – PPS

- No Load transition overshoot settling time for APDO
 - Same reasoning as for Fixed Supply
- tPpsCLProgram tPpsCVCLTransient tPpsCLSettle min limit removal:
 - Removes the minimum settling time limitation for implementations with fast settling time. Feedback from implementers and compliance testing indicated limitation not necessary
- Relaxed iPpsCLOperating to enable better Sink fast charging algorithms:
 - Clarify the measurement points (e.g. the beginning and end points)
 - Widen the negative allowance from 0 to -25 mA (1/2 current step)
 - Clarify that the load has a positive allowance and sets the allowance to +25 mA
- Clarify vMin Shutdown Voltage Threshold:
 - PPS required to shut down Vbus when output voltage < vMin
 - Defined shutdown voltage as less than ~90% of vMin

Charging – Multi-port

- Testing
 - BIST Shared Capability Test Mode – forces shared capacity ports to offer full capabilities
 - Port identification – Ports return a unique port number (not a USB port number!)
- Source Capabilities requirements for multi-port systems
 - Source capabilities can be sent if system power has changed even if port capabilities are the same
 - Removes need to work out if a particular port power has changed
- Require Sinks support Sink Capabilities Extended
 - Enables multi-port systems to better manage power based on Sink needs
 - Extended Capabilities contain min, operating and maximum power numbers

USB4™

- Discover Identity for DFP/UFP/DRD
 - New VDOs added for use by DFP, UFP and DRD products
 - Capability to identify USB4 products
- Discover Identity additions for cables
 - Capability to identify USB4 cables
- Enter USB
 - Mandatory entry mechanism for USB4 on Ports and Cables
 - May also be used to enter USB 3.2 and USB 2.0 operation
- Data Reset
 - Means to reset the USB data connection between PD Ports
 - Resets the cable by power cycling VCONN
 - Does not affect the power contract or data/power roles

Cables

- Cable SOP Assignment to Fixed
 - SOP'/SOP'' assigned at time of manufacture
 - Prevents issues relating to assignment based on VCONN Source and presence of Ra
 - Dynamic assignment not required by known alternate modes
- Cable Plug Get_Manufacturer_info Clarification
 - Clarify response when Manufacturer Information not supported by a cable (ignore)
- Re-add speed field for compatibility
 - Responded to interoperability issues by restoring the speed field in VDO 1

Fast Role Swap

- Checking Sink Capabilities for Fast Role Swap
 - Initial Sink (e.g. Laptop) required to request sink capabilities from initial sources (e.g. Hub)
 - Checks for FR_Swap support and power requirements
 - Initial sink does not respond to FR_Swap signalling when:
 - The capabilities are not requested from the initial source.
 - FR_Swap is not supported by the initial source
 - Initial sink is unable to provide the requested FR_Swap power

Table 6-14 Fixed Supply PDO - Sink

Bit(s)	Description										
B31...30	Fixed supply										
B29	Dual-Role Power										
B28	Higher Capability										
B27	Unconstrained Power										
B26	USB Communications Capable										
B25	Dual-Role Data										
B24...23	Fast Role Swap required USB Type-C Current (see also [USB Type-C 2.0]): <table border="1"><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>00b</td><td>Fast Swap not supported (default)</td></tr><tr><td>01b</td><td>Default USB Power</td></tr><tr><td>10b</td><td>1.5A @ 5V</td></tr><tr><td>11b</td><td>3.0A @ 5V</td></tr></tbody></table>	Value	Description	00b	Fast Swap not supported (default)	01b	Default USB Power	10b	1.5A @ 5V	11b	3.0A @ 5V
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00b	Fast Swap not supported (default)										
01b	Default USB Power										
10b	1.5A @ 5V										
11b	3.0A @ 5V										
B22...20	Reserved - Shall be set to zero.										
B19...10	Voltage in 50mV units										
B9...0	Operational Current in 10mA units										

Power Role Swap

- Source Caps from Sink clarification
 - Sink responds to a Get Source Caps Request with its full Capabilities regardless the cable capabilities.

Miscellaneous Updates

- tRetry relaxation
 - Increased tRetry (max) from 75 μ s to 195 μ s.
 - Value 195 μ s was chosen to align with tTransmit
- Respond to invalid target in received Get_Manufacturer_Info message by:
 - Setting Manufacturer String to “Not Supported”
 - VID to 0xFFFF
 - PID to 0x0000
- Country Codes and Country info messages shortened
 - Restricting to 26 bytes ensures that only one chunk is returned
 - Support for chunked messages is not needed
- Protocol Errors During Startup particularly for Cable Discovery
 - Define Soft Reset operation when protocol errors occur and there is no Explicit Contract
- Improve VPD definition
 - Applicability of messages to VPDs added
 - Current for VPD charge-through devices added to VPD VDO

Time for Q&A

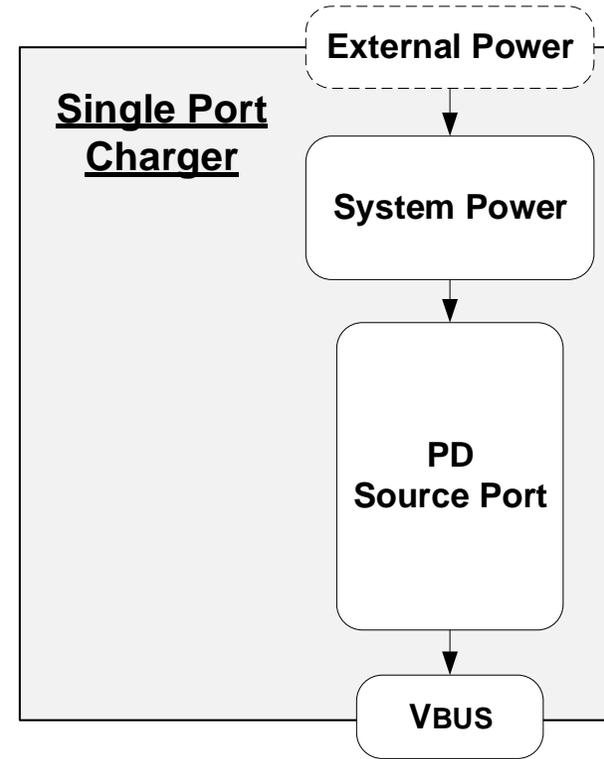
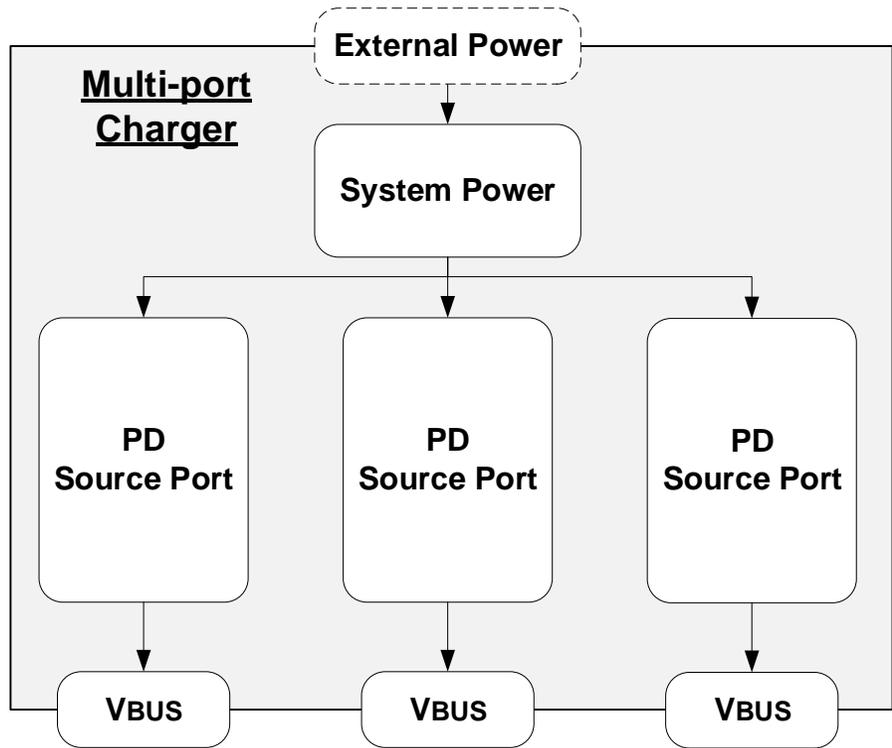
Presentation Agenda

- Introduction
- **Charging**
- USB4™
- Compliance

Charging

- **Overview**
- Fixed Supply
- PPS
- Multi-port
- Good to know

Charger Configurations



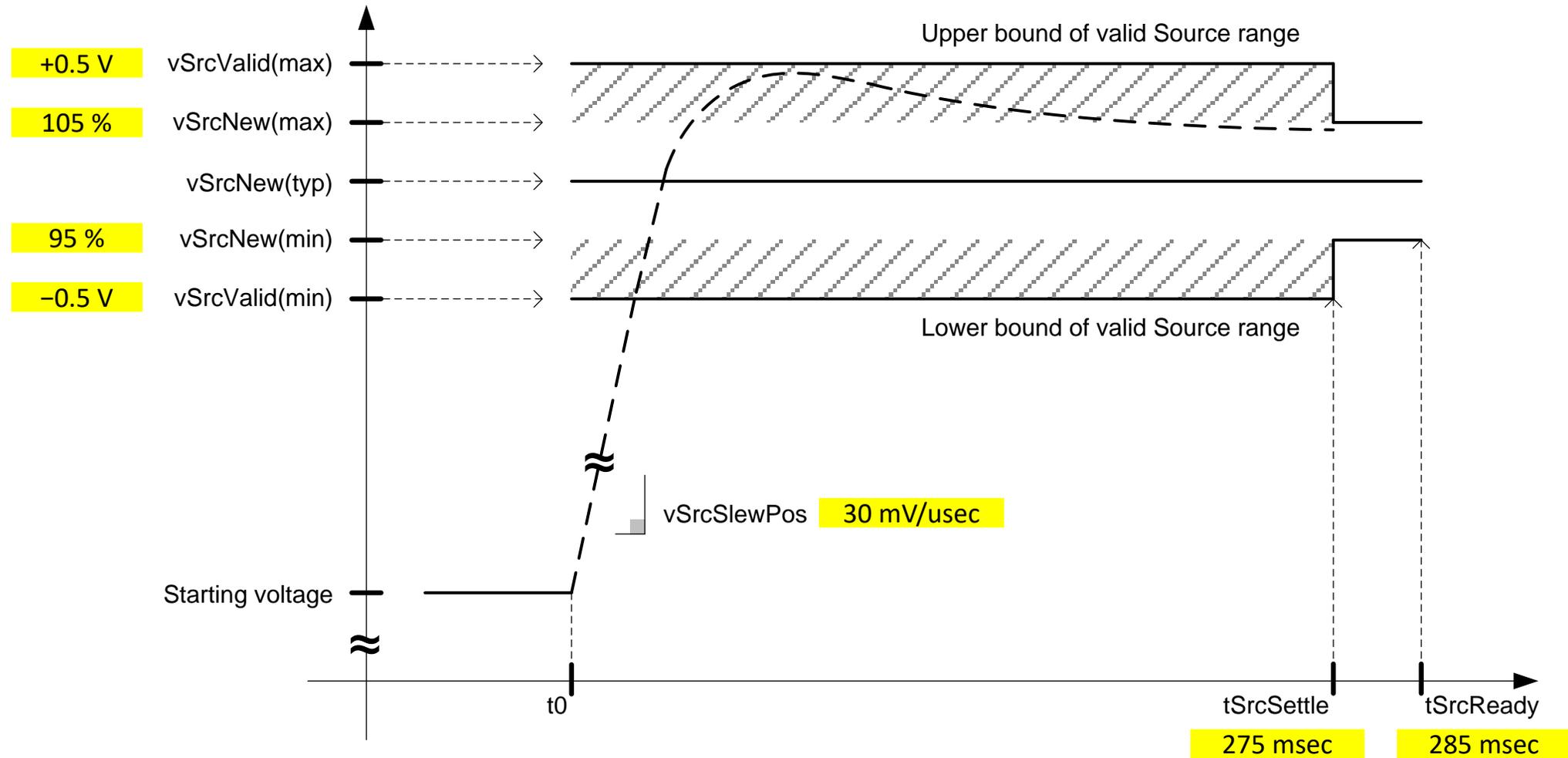
Fixed Sources & Programmable Power Sources

Aspect	Fixed Source	Programmable Power Source
<i>Constant Voltage mode (refer to Chapter 10)</i>	5 V 9 V 15 V 20 V	5V Prog (3.3 V to 5.9 V) 9V Prog (3.3 V to 11.0 V) 15V Prog (3.3 V to 16.0 V) 20V Prog (3.3 V to 21.0 V)
<i>Current</i>	Round(PDP/Voltage) to nearest 10mA	RoundDown(PDP/Prog Voltage) to nearest 50mA
<i>Step Size</i>	None	Nominal 20 mV
<i>Current Limit mode</i>	None	Yes, nominal 50 mA steps
<i>Periodic RDOs during operation</i>	No – does not apply	Yes, needed for PPS operation
<i>Requires Robust Port Design</i>	Yes	Yes

Charging

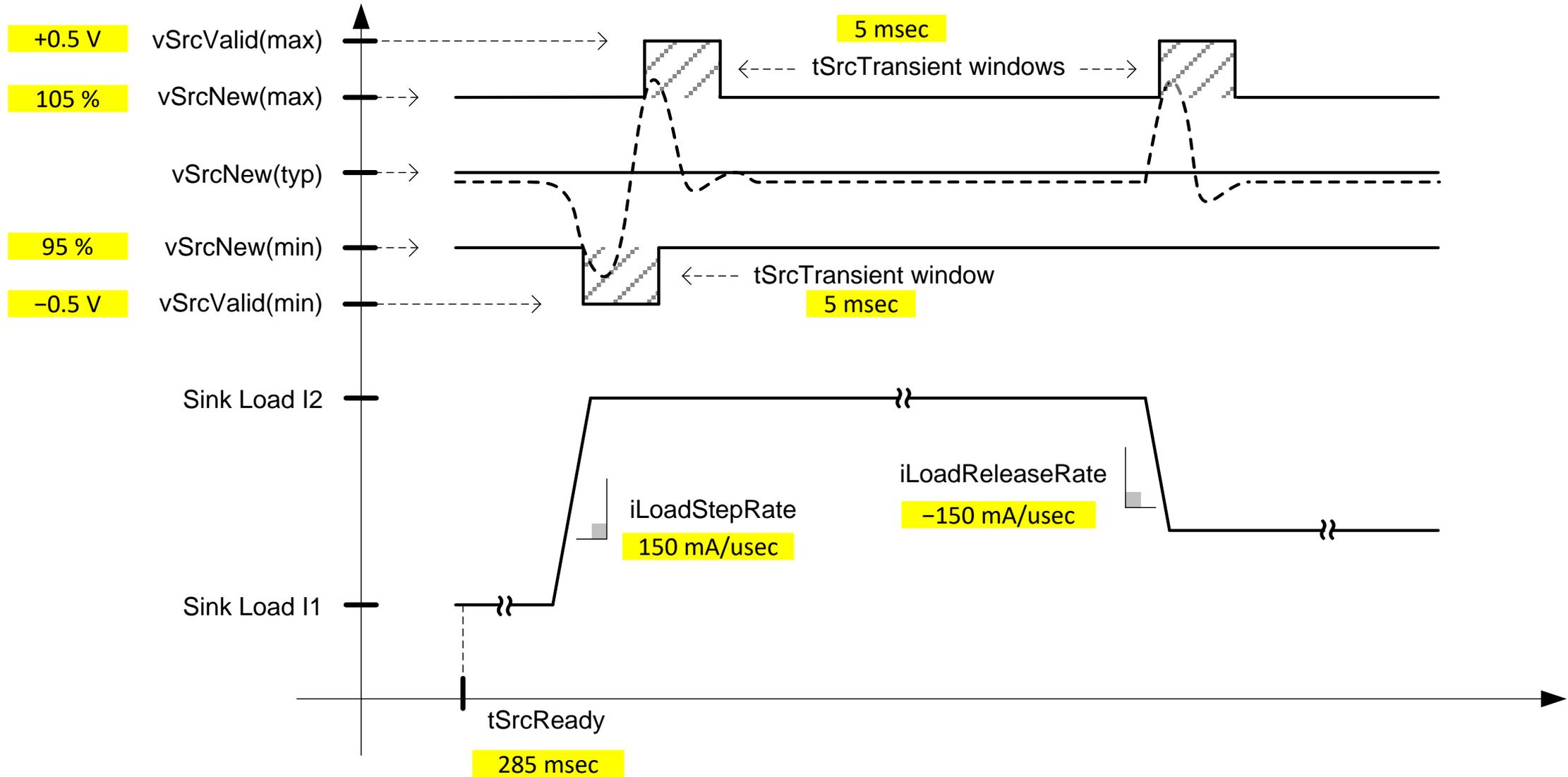
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Source Positive Transitions

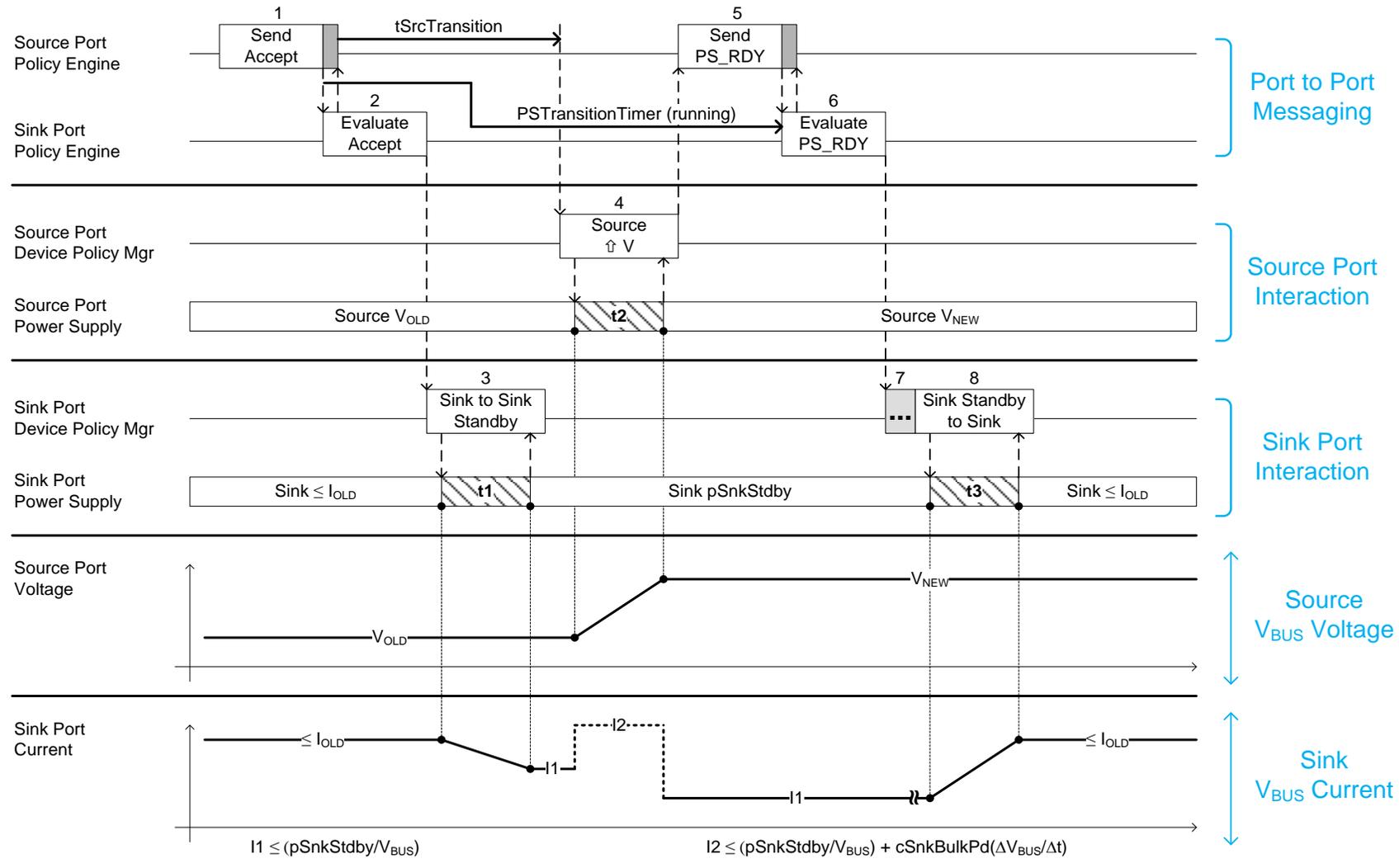


- The voltage limits do not apply to v_{Safe0V} and v_{Safe5V}

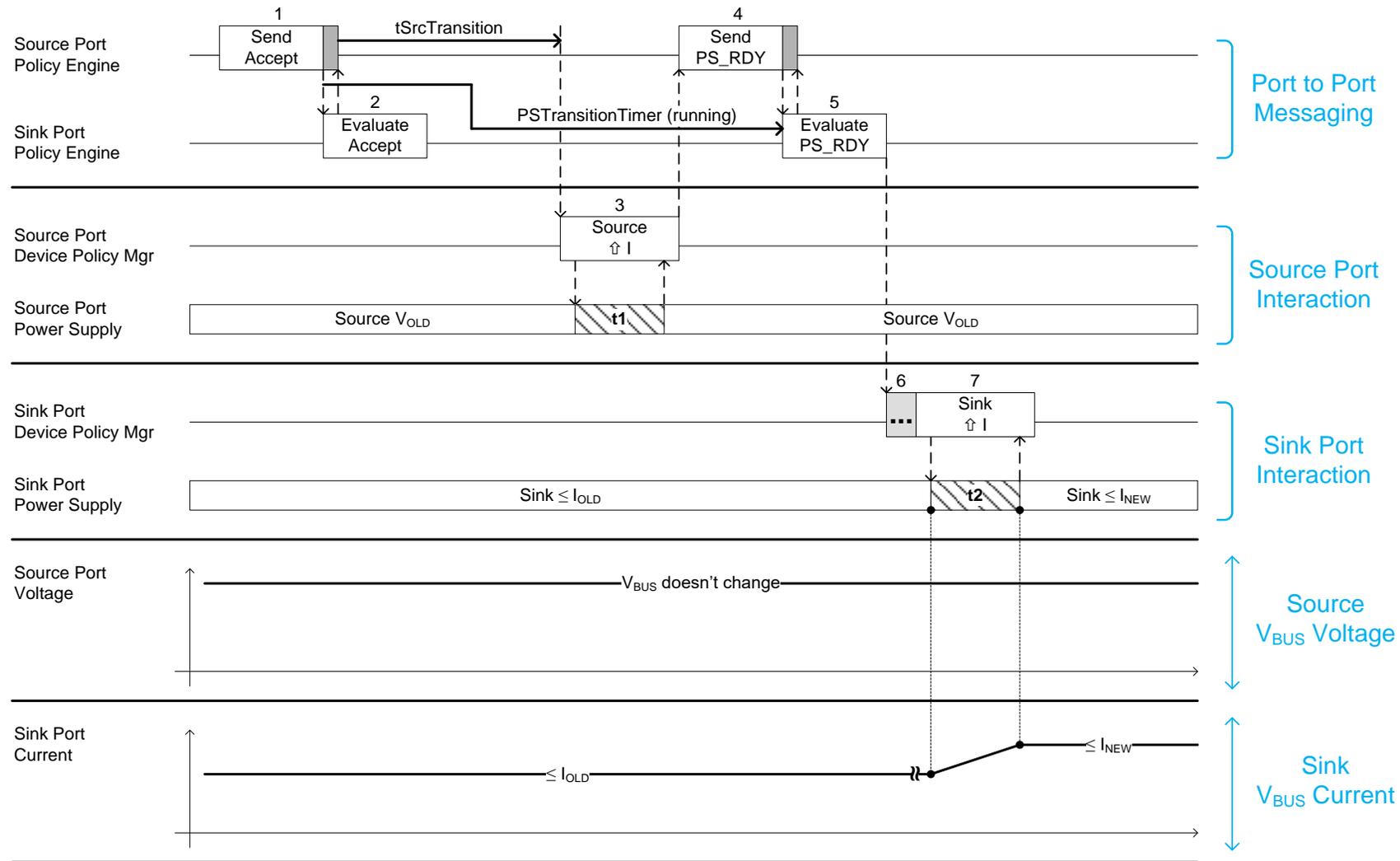
Application of vSrcNew & vSrcValid after tSrcReady



Transition to Increase Voltage



Transition to Increase Current



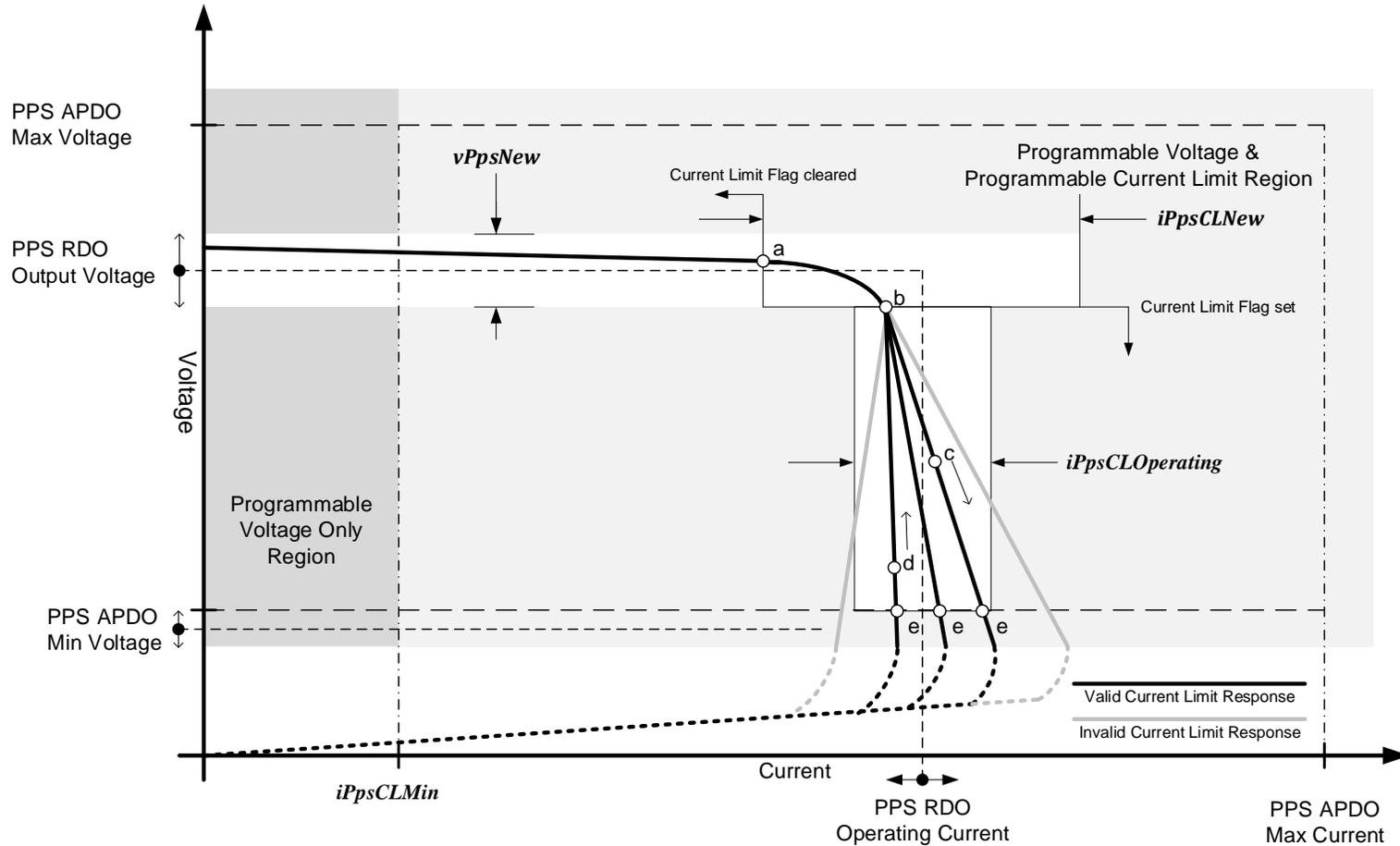
Charging

- Overview
- Fixed Supply
- **PPS**
- Multi-port
- Good to know

What is Programmable Power Supply (PPS)

- Sink Directed Power Source
 - The Source output voltage adjustable in 20 mV steps
 - The Source output current limit adjustable in 50 mA steps
- Constant voltage operation when the Sink draws less than RDO Operating Current
- Source current limit operation when the Sink draws more than RDO Operating Current
 - Current Limit mode is used for normal operation, not for protection
 - Over-current protection needs to be additionally added
- Power Limit mode can be optionally supported
 - Source limits output power to \leq PDP
 - Reduces the voltage to maintain power level as current increases

PPS = Programmable Voltage + Current Limit

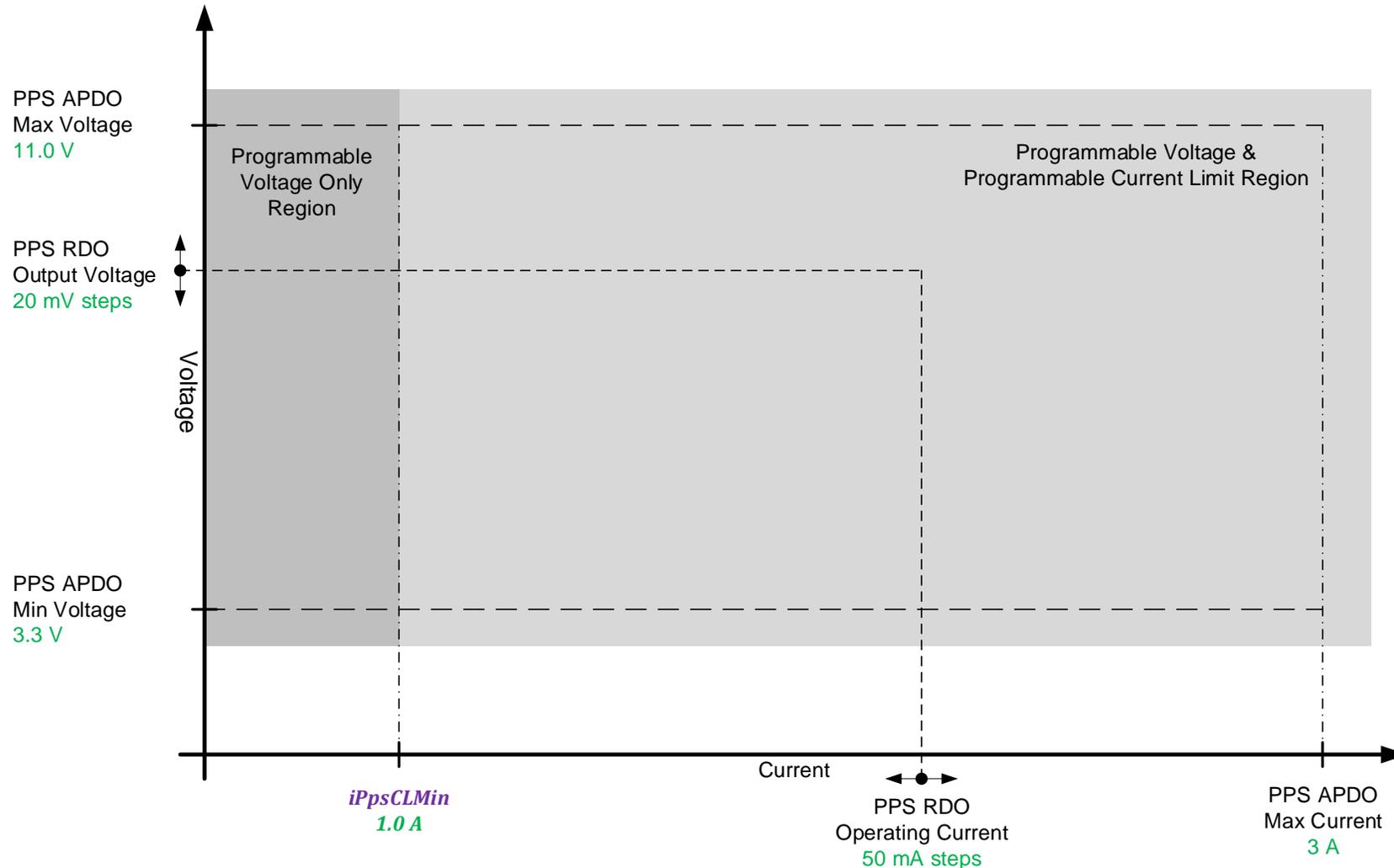


- Shaded areas indicate:
 - Max and min nominal output voltage
 - Max and min operating current
 - Values in PPS APDO including tolerance
- PPS APDO Min Voltage is the same value across all of the APDOs
- Sloped line indicates the PPS load regulation characteristic

Coming to Terms with PPS

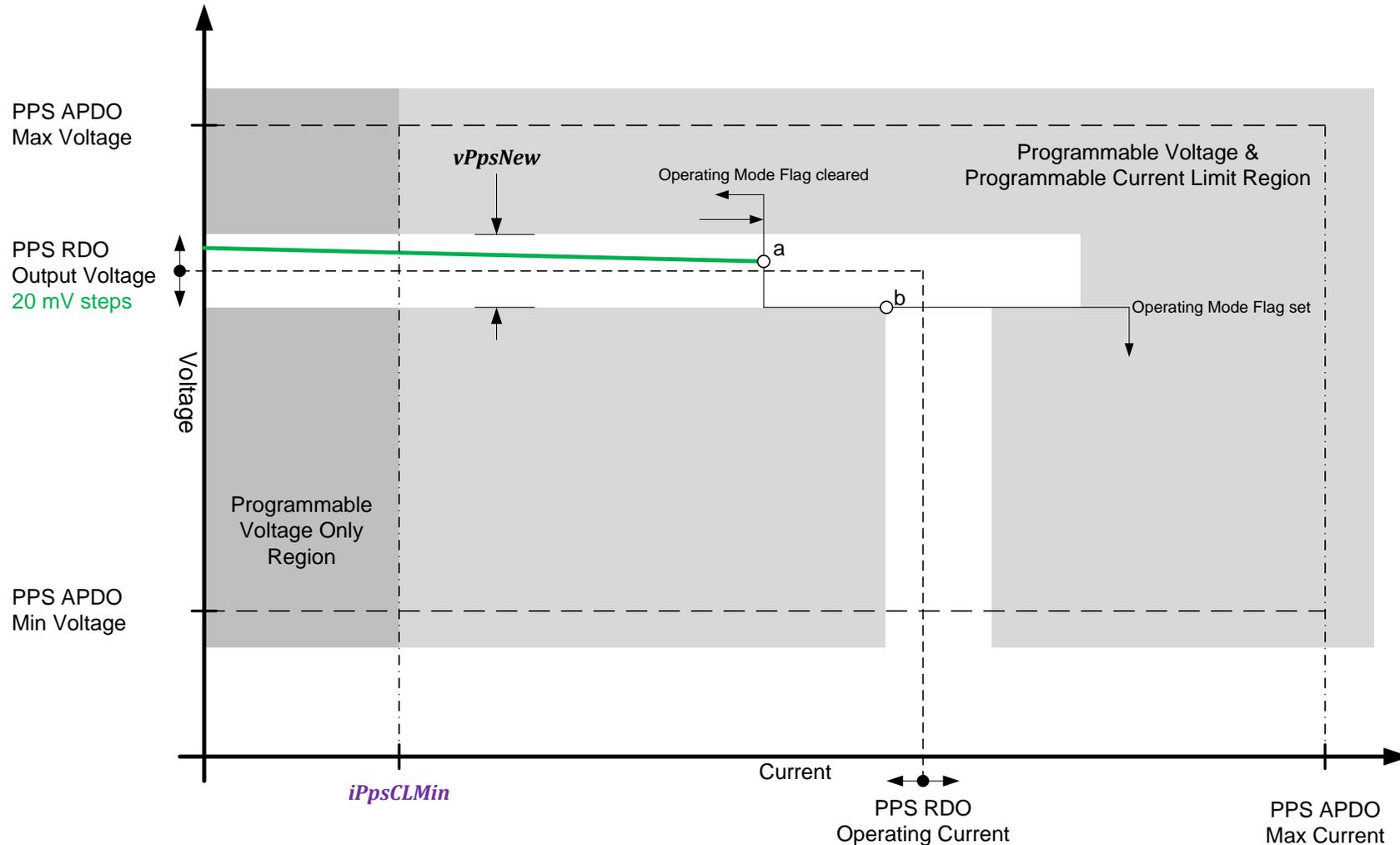
- X-axis
 - $i_{PpsCLMin} = 1 \text{ A}$
 - PPS RDO Operating Current = Requested current level
 - PPS APDO Max Current = Maximum current based on PDP
- Y-axis
 - PPS APDO Min Voltage = Min voltage which is 3.3 V regardless of PDP
 - PPS RDO Output Voltage = Requested voltage level
 - PPS APDO Max Voltage = Max voltage which is defined by PDP

Example: PDP = Prog9V, PDP = 27 W



- PPS RDO Output Voltage step size is fixed at 20 mV nominal
- PPS RDO Operating Current step size is fixed at 50 mA nominal
- Min and max PPS range are defined by the PPS APDO
- Output voltage and operating current of the PPS is defined by the PPS RDO
- Current limiting is not defined for PPS APDOs or PPS RDOs below 1 A

Constant Voltage Segment of the PPS Curve



- The PPS RDO output voltage step size is fixed at 20 mV nominal
- The PPS RDO output voltage can be changed in single-bit or multiple-bit steps
- PPS output voltage regulation occurs to the left of the point designated as (a)
- The v_{PpsNew} tolerance is $\pm 5\%$

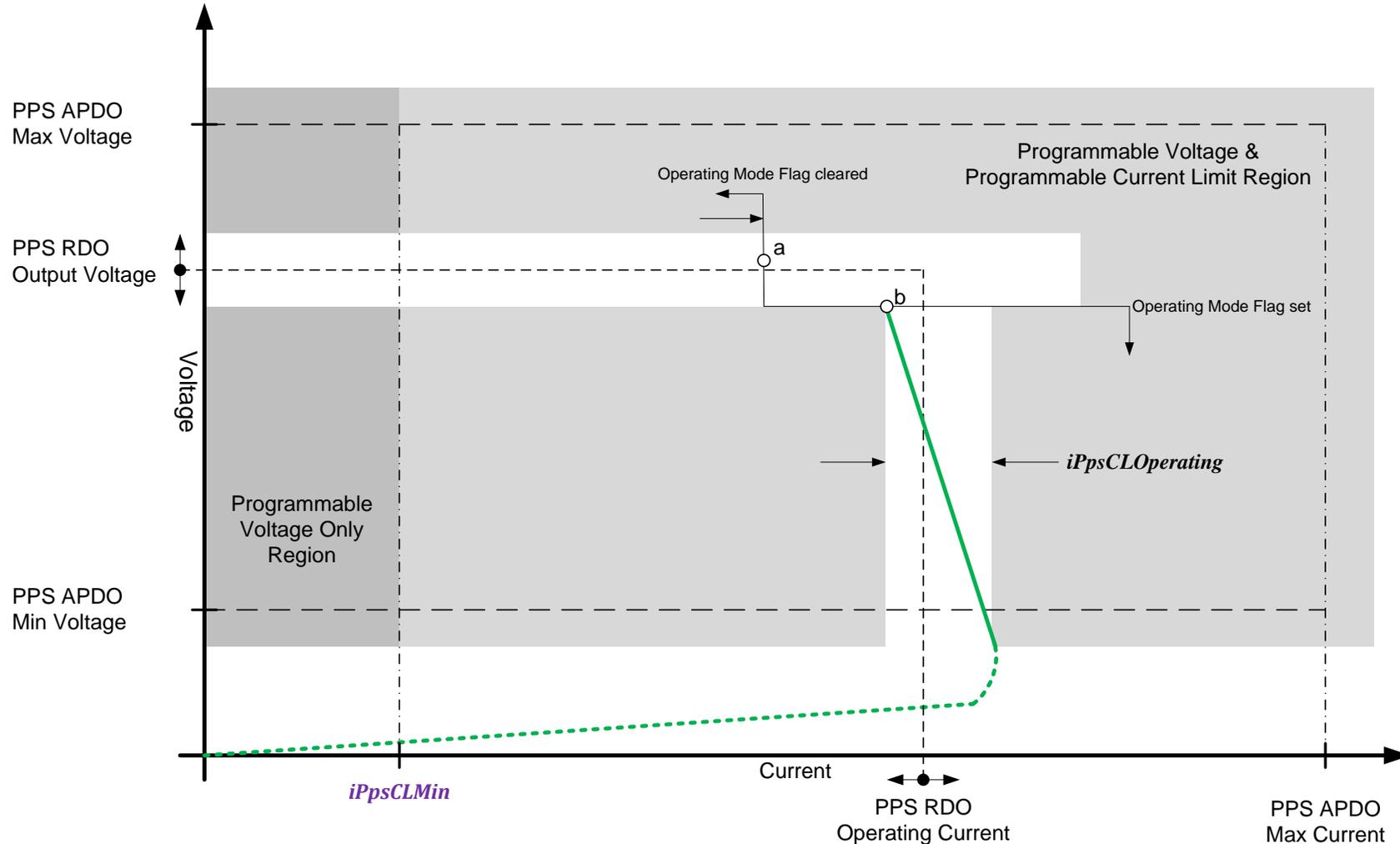
Constant Voltage Tolerance, Step Size & Monotonicity

- The regulation tolerance is $\pm 5\%$
- The Constant Voltage RDO steps size is 20 mV nominal

Example:

- RDO Output voltage = 4.0 V, the valid regulated range is 3.8 V to 4.2 V
- +1 LSB change of RDO increases the output voltage by 20 mV nominal
 - A non-positive change of the output voltage in response to +1 LSB change of RDO violates the monotonicity requirement

Current Limit Segment of the PPS Curve

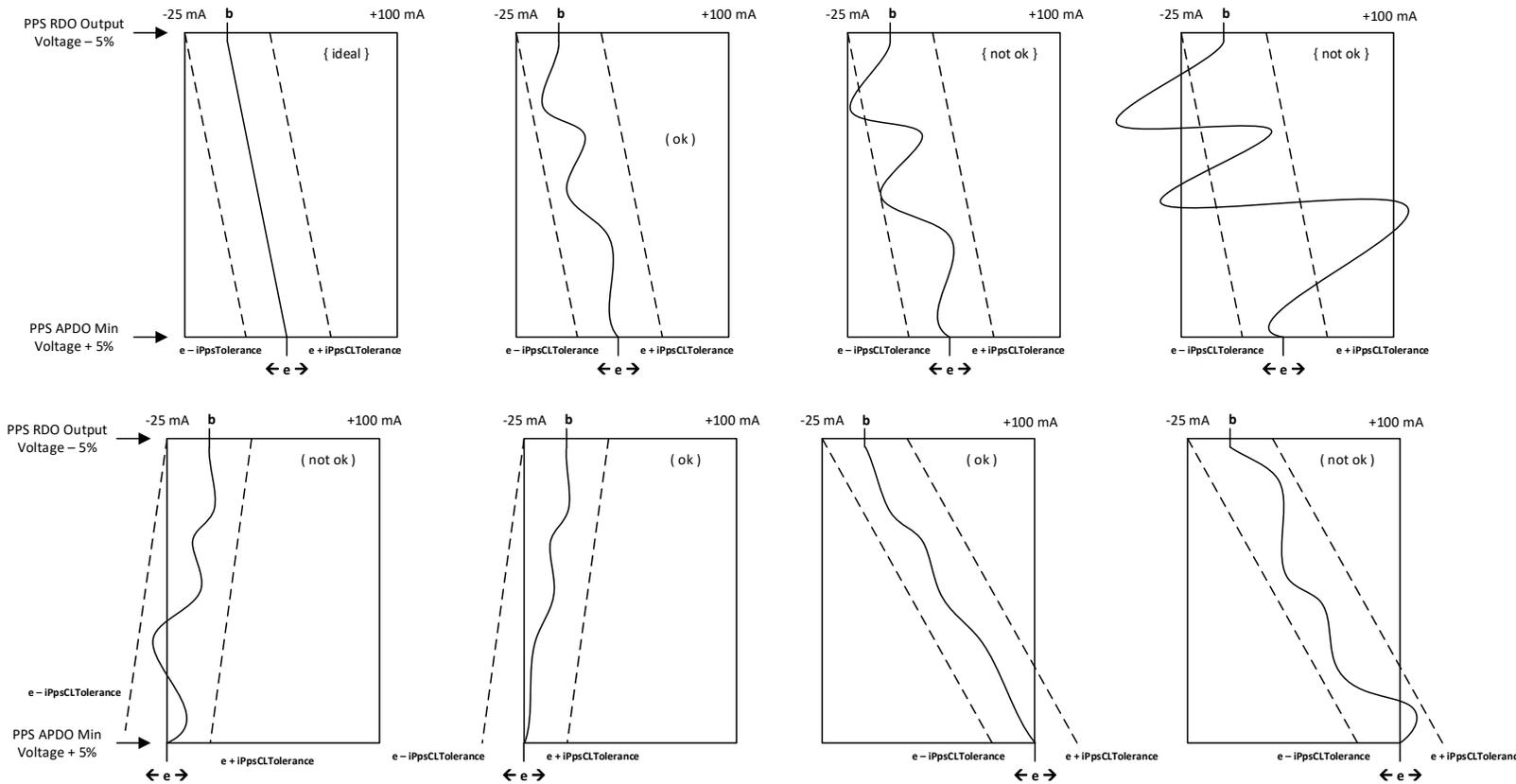


- PPS shall exhibit a current limit response like the one shown in the diagram
- PPS is not required to provide power for voltages below the PPS APDO Min Voltage, including tolerance
- PPS output current limiting shall occur below the point designated as (b)

PPS Current Limit – Current Parameters

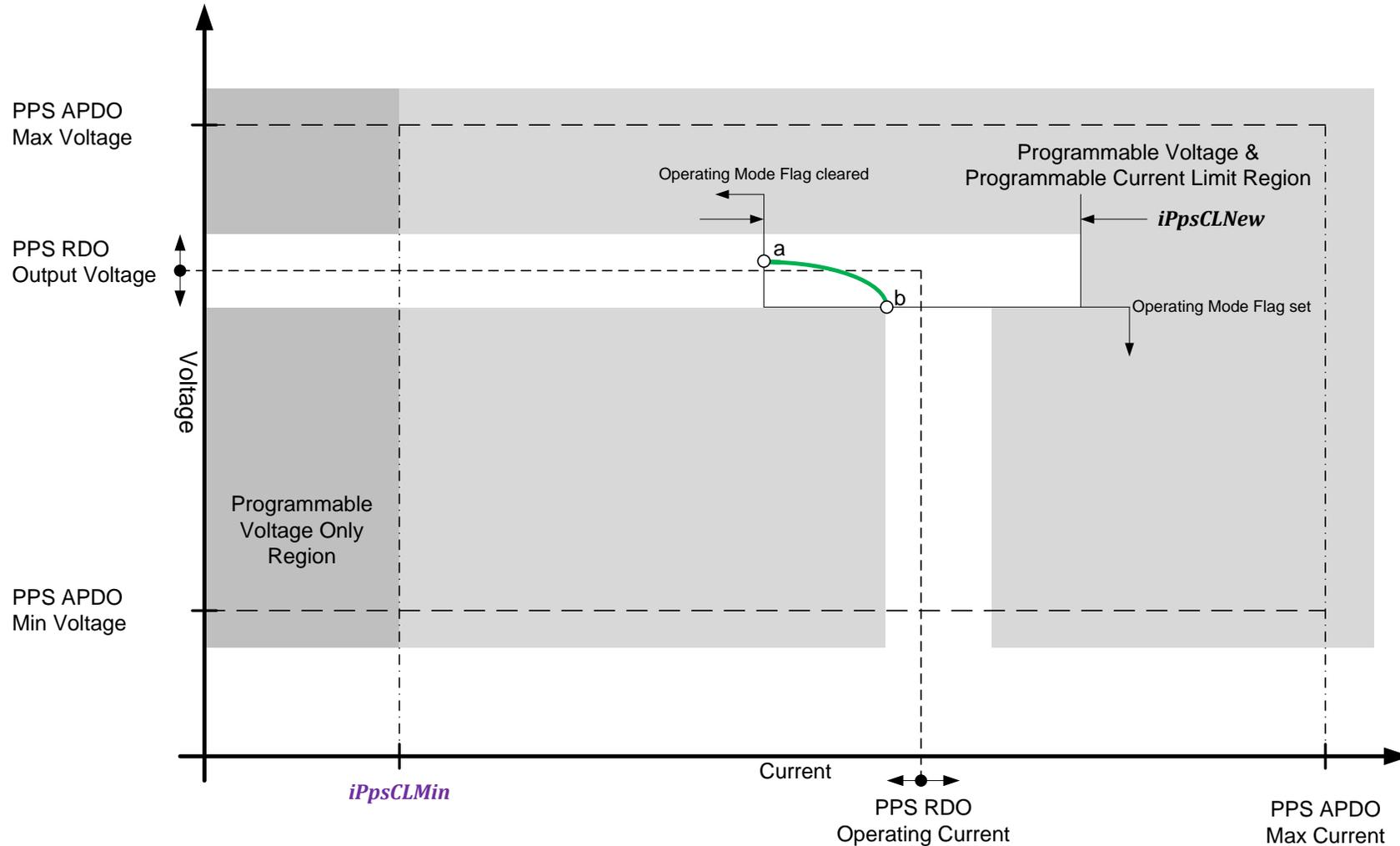
<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Description</i>
iPpsCLMin	1			A	Current Limit mode is only required when the PPS RDO Operating current is above 1 A.
iPpsCLNew	-150		+150	mA	Current Limit mode accuracy when the PPS RDO Operating Current is 1 A or greater and 3 A or less.
	-5		+5	%	Current Limit mode accuracy when the PPS RDO Operating Current is greater than 3 A.
iPpsCLOperating	-25		+100	mA	Range beyond iPpsCLNew over which the current can vary during Current Limit mode.
iPpsCLStep		50		mA	Nominal output current change for every LSB change of PPS RDO Operating Current.
iPpsCLTransient	New load - 100		New load + 100	mA	Range over which the current can vary during a load transient which does not cause a transition out of Current Limit mode.
iPpsCvCLTransient	iPpsCLNew - 100		New load + 500	mA	Range over which the current can vary during a load transient which causes a transition from Constant Voltage mode to Current Limit mode.

Good versus Bad PPS Current Limit Response



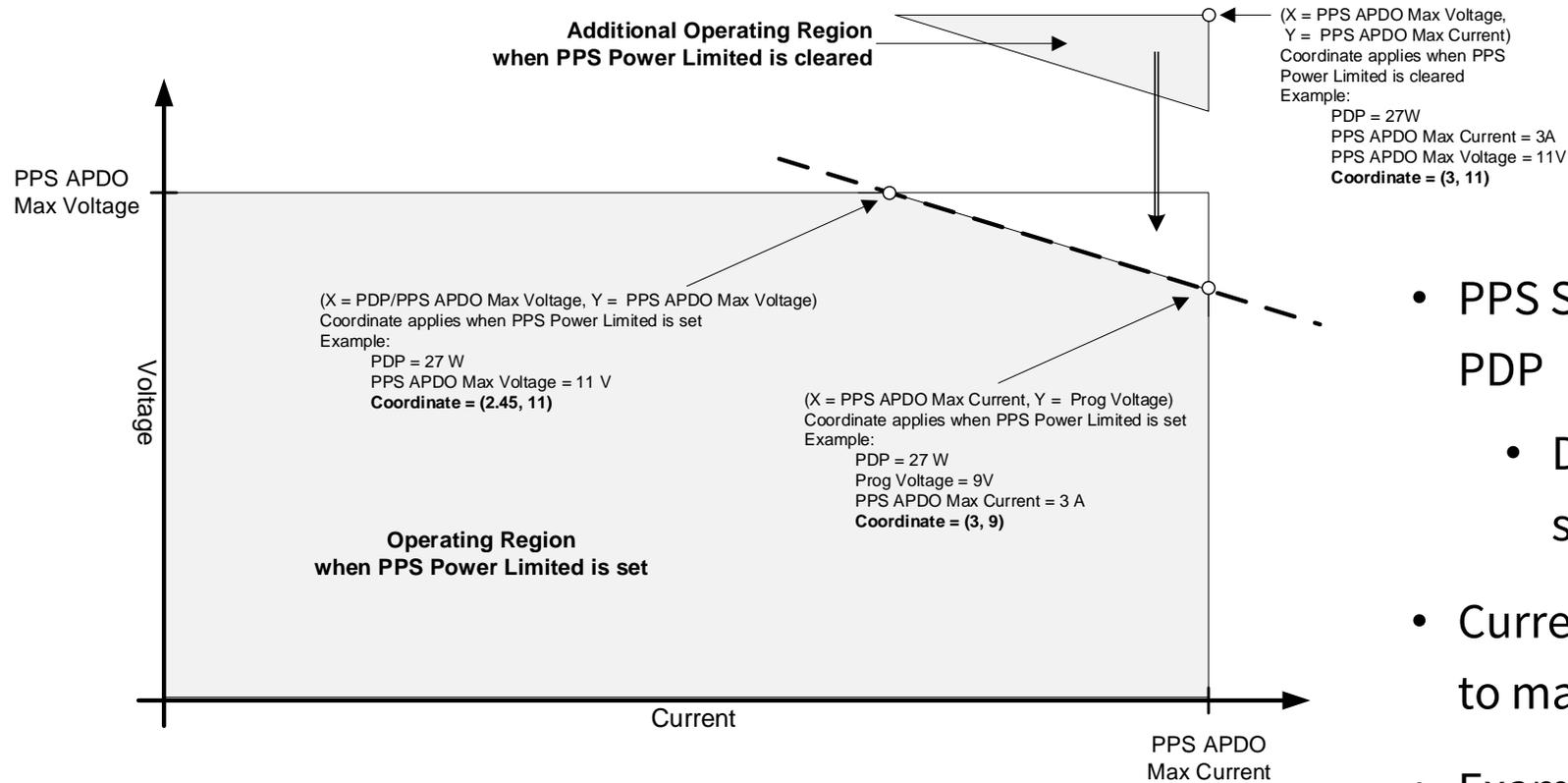
- A current limit response that goes outside of the $iPpsCLOperating$ band is not allowed
- A current limit slope where voltage decreases with decreased load current is not allowed
- Current limit responses do not need to span the entire $iPpsCLOperating$ band from left to right

Constant Voltage to Current Limit and Back



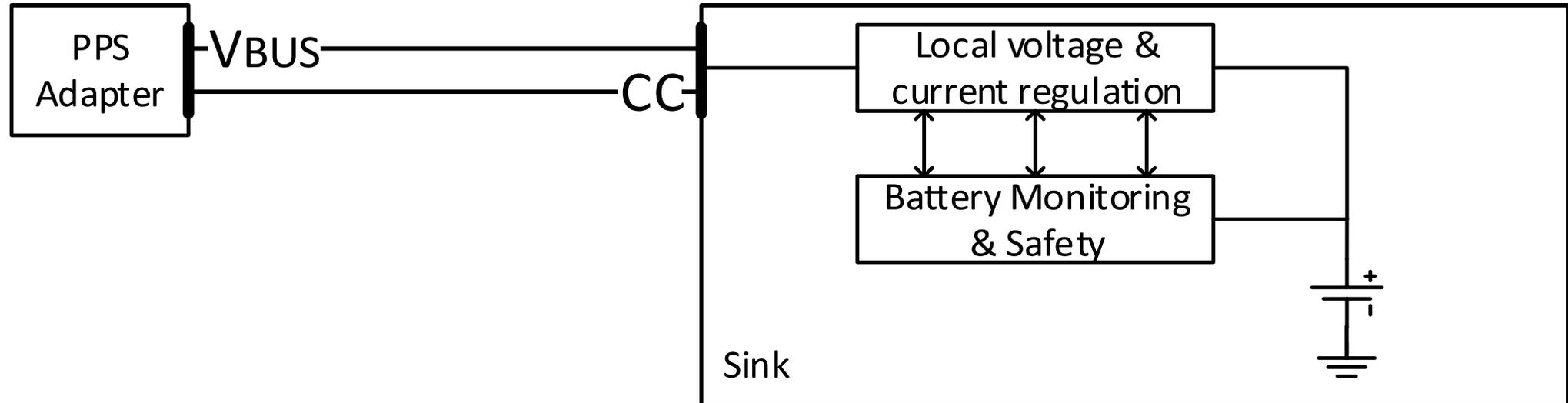
- Left of point (a) the PPS output current is below the tolerance band for a given PPS RDO Operating Current therefore is in **Constant Voltage mode**
 - Operating Mode Flag is cleared
- Below point (b) the PPS output voltage is below the tolerance band for a given PPS RDO Output Voltage therefore is in **Current Limit mode**
 - Operating Mode Flag is set
- The state of the Operating Mode Flag between points (a) and (b) is not defined and the operational mode is unknown

Power Limited Mode



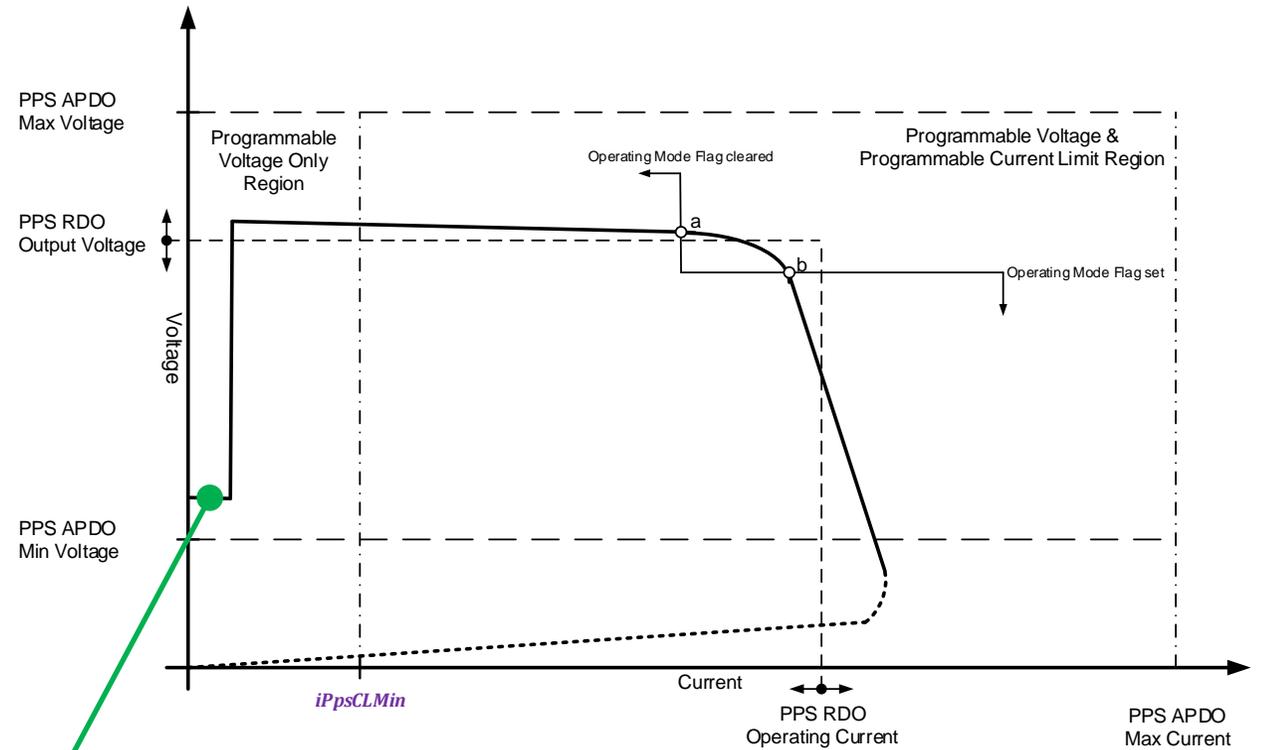
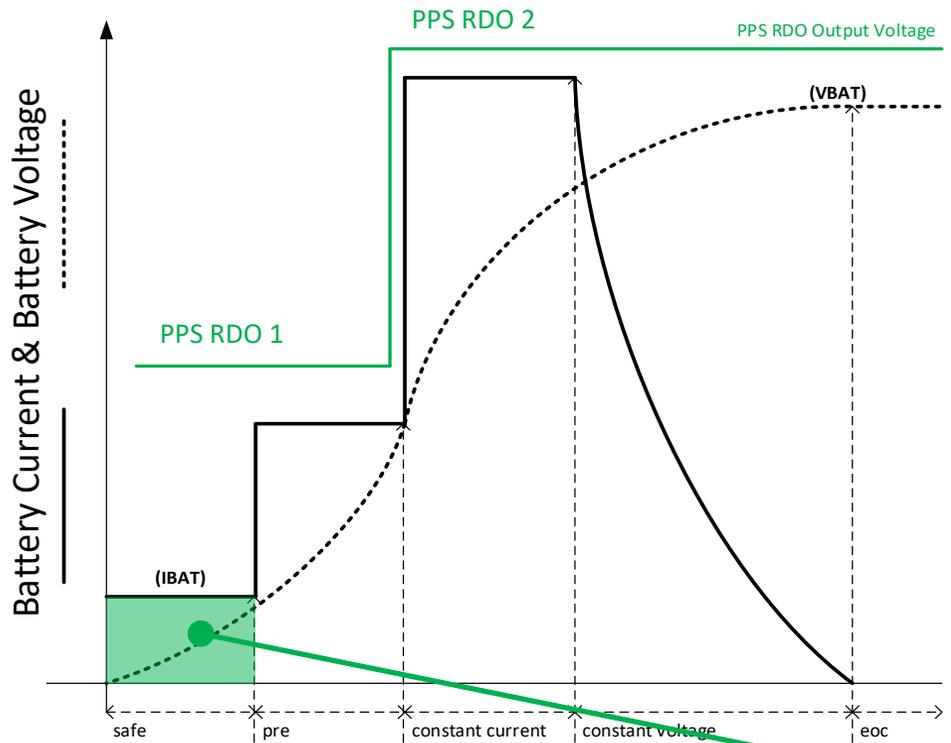
- PPS Source limits its output power to the PDP
 - Defined in design; cannot be selected by the Sink
- Current held constant; voltage lowered to maintain PDP
- Example a PPS charger rated at 27 W:
 - Not power limited maxes out at 33 W
 - Power limited maximum is 27 W

PPS Charging Example



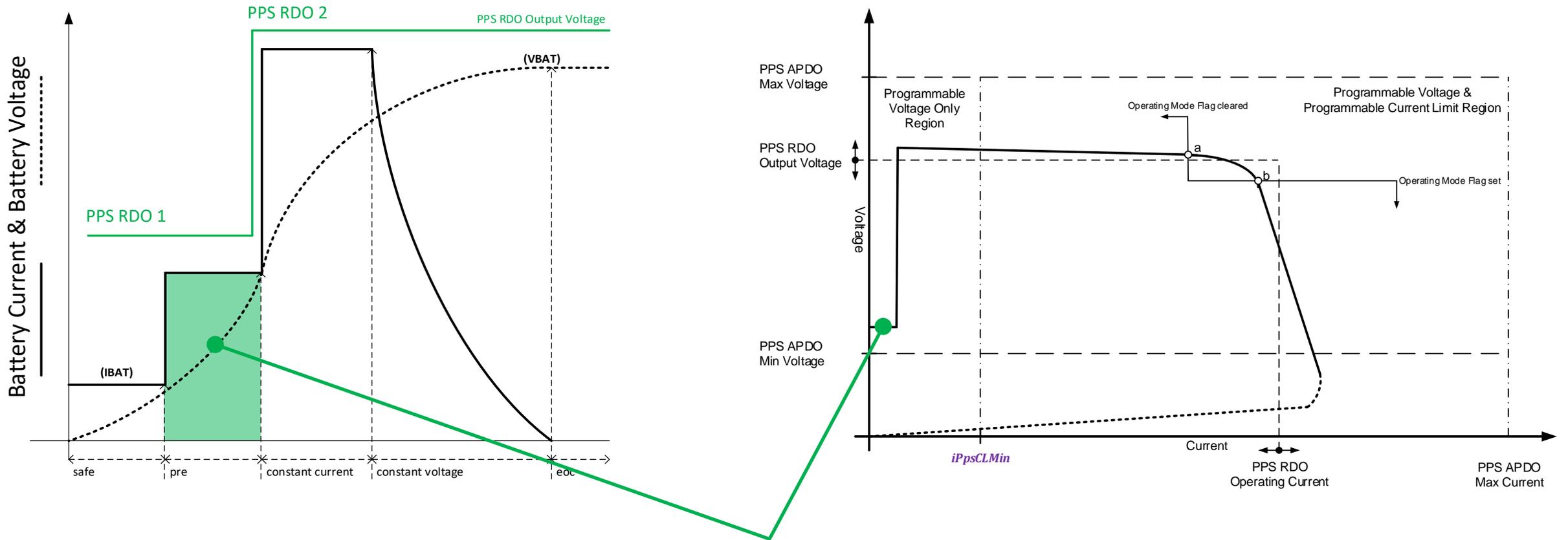
- Conceptually the Sink controls the PPS to charge its battery
- The Sink sends periodic RDOs to keep-alive the Source 'you must'
- In practice, the Sink must provide local regulation and battery protection

Safe Charge



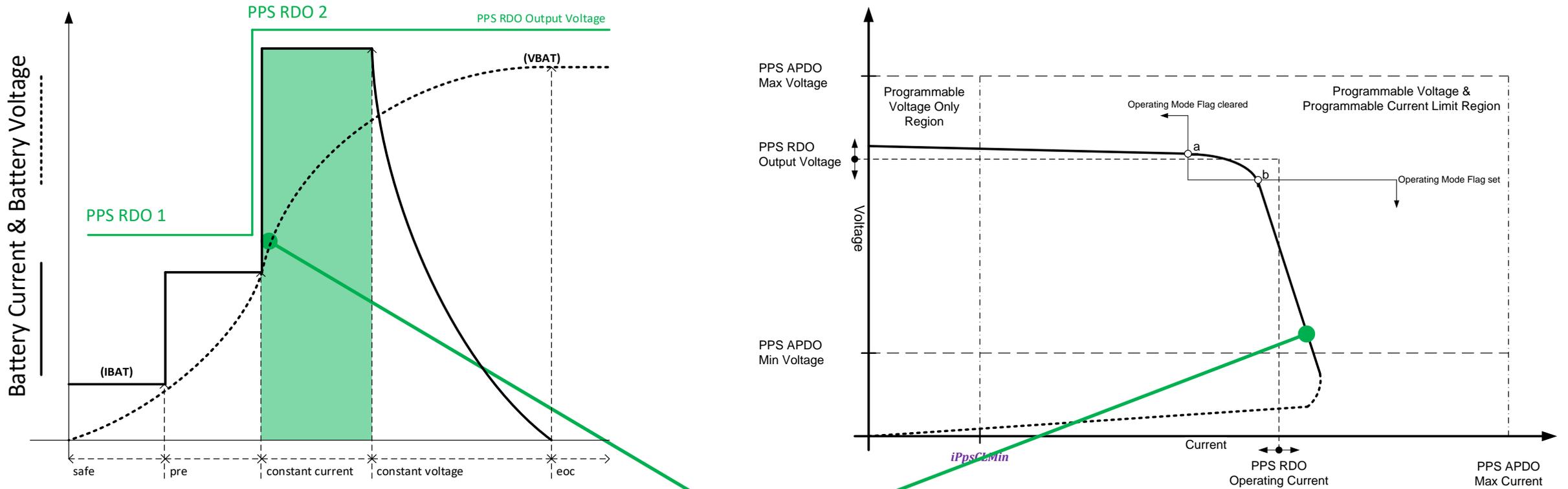
LOW battery current & LOW battery voltage
PPS in Constant Voltage mode
Operating Mode Flag is cleared

Pre Charge



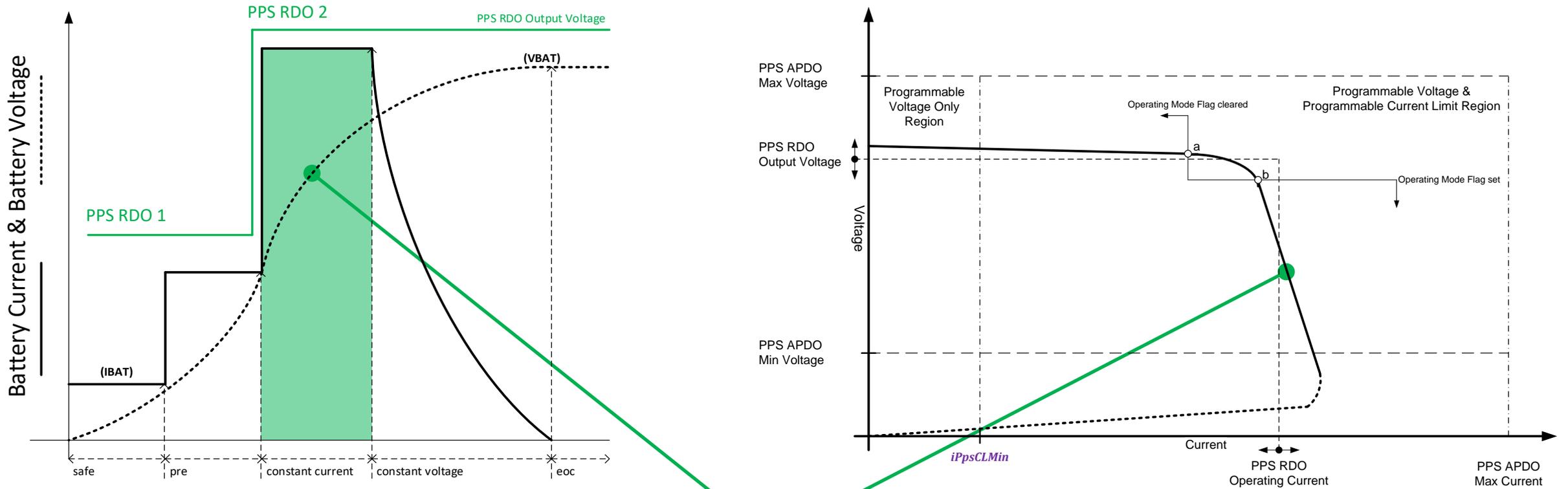
LOW charging current & LOW battery voltage
PPS in Constant Voltage mode
Operating Mode Flag is cleared

Start of CC Charge



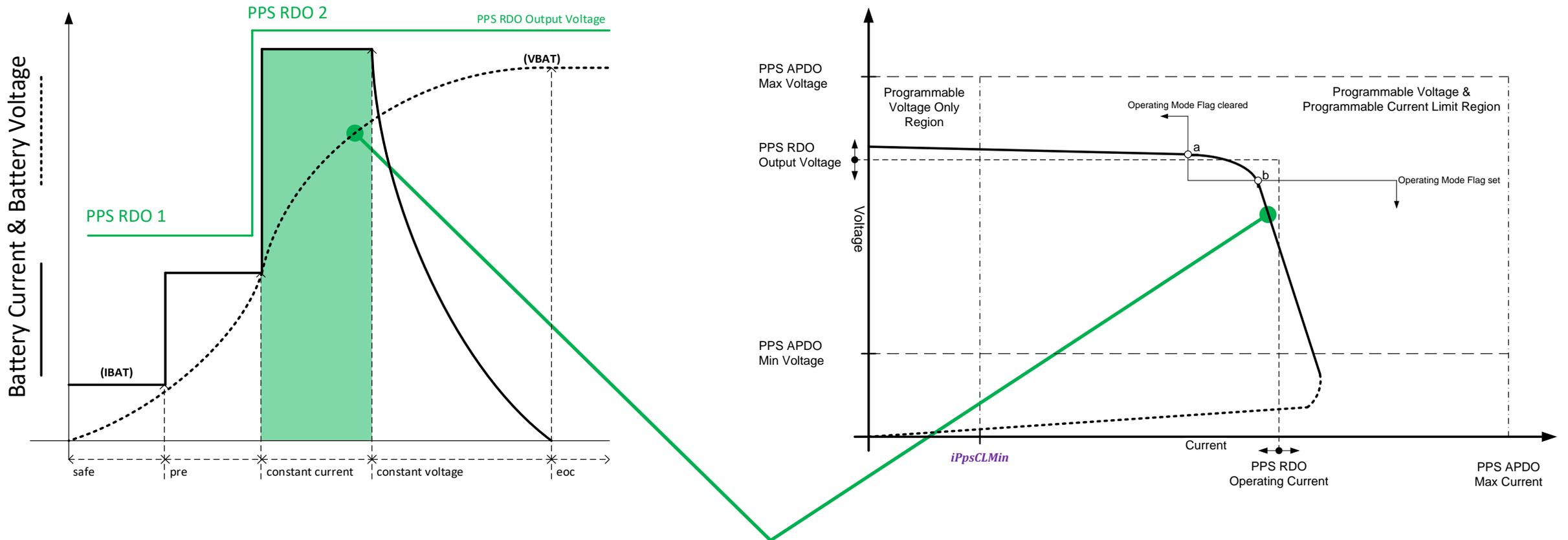
HIGH charging current & LOW battery voltage
PPS in Current Limit mode
Operating Mode Flag is set

Progressing through CC Charge



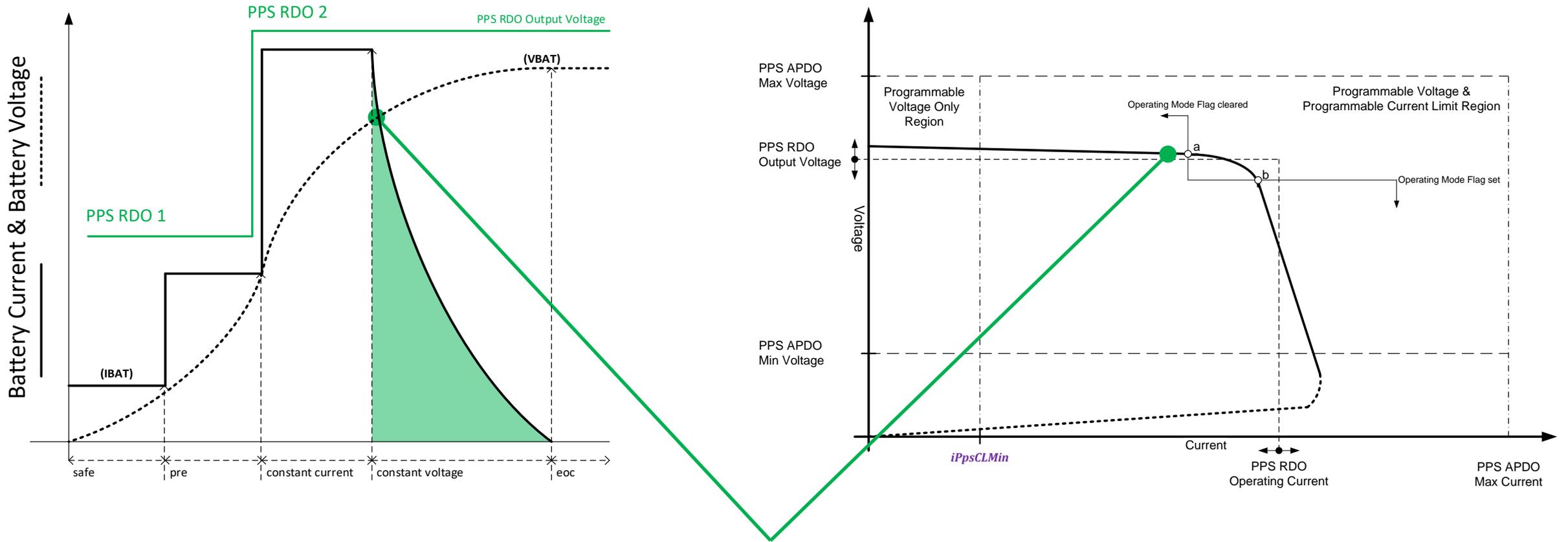
HIGH charging current & INCREASING battery voltage
PPS in Current Limit mode
Operating Mode Flag is set

Nearing the End of CC Charge



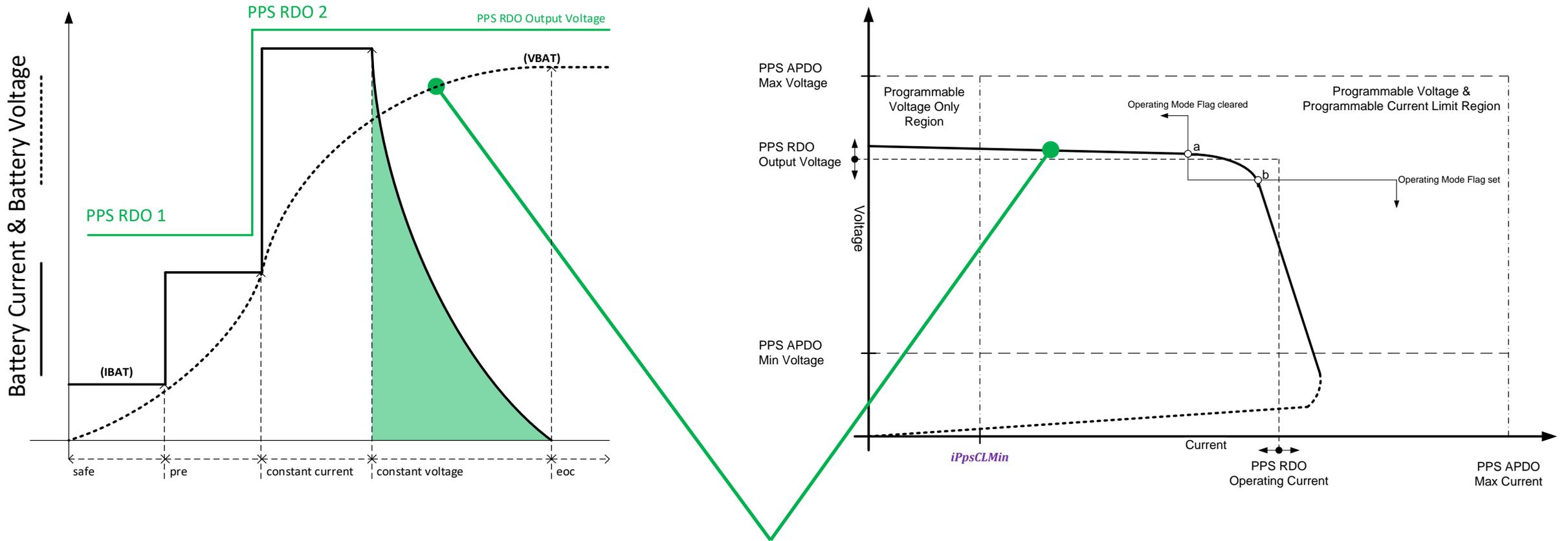
HIGH charging current & HIGH battery voltage
PPS in Current Limit mode
Operating Mode Flag is set

Start of CV Charge



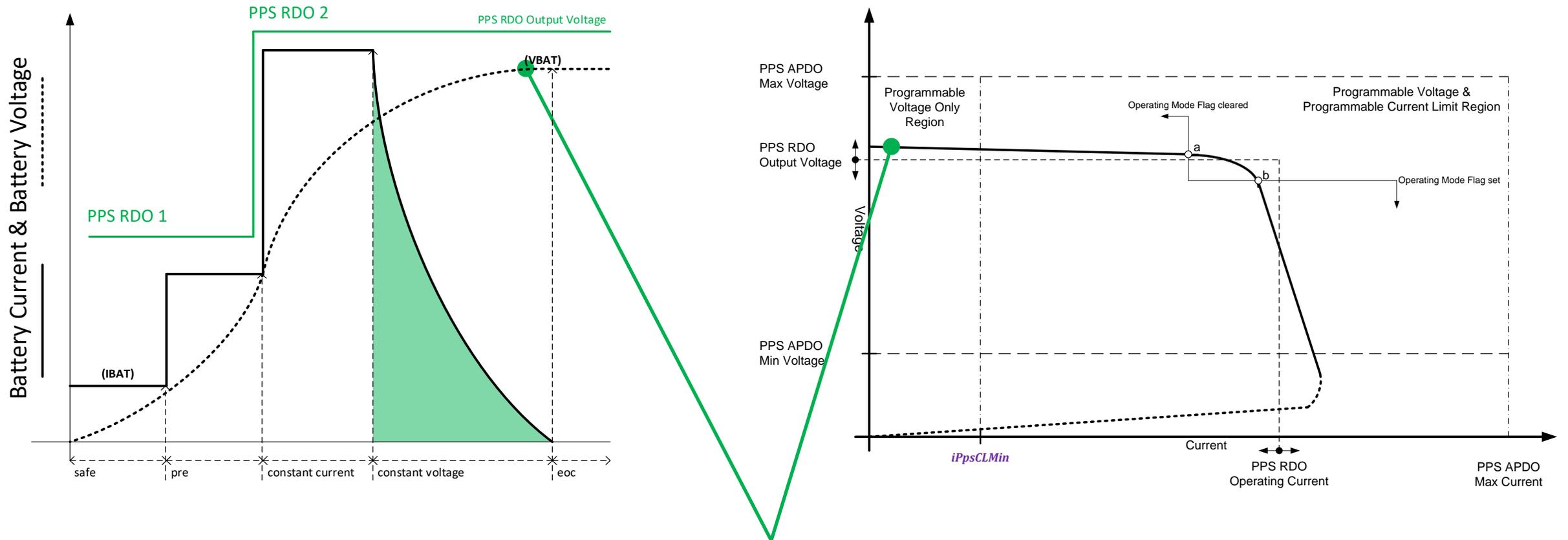
HIGH charging current & HIGH battery voltage
PPS in Constant Voltage mode
Operating Mode Flag is cleared

Progressing through CV Charge



DECREASING charging current & **HIGH** battery voltage
PPS in Constant Voltage mode
Operating Mode Flag is cleared

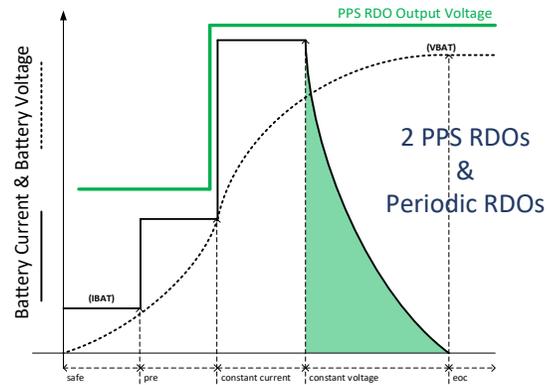
Nearing the End of CV Charge



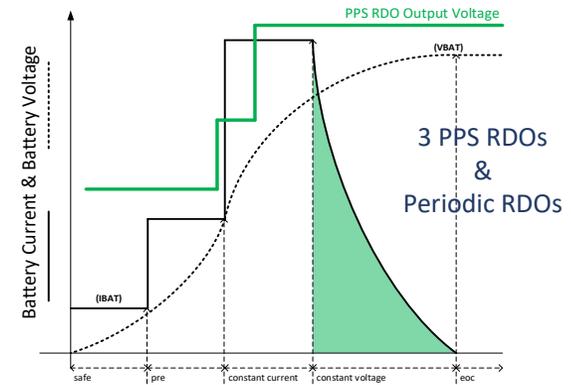
LOW charging current & HIGH battery voltage
PPS in Constant Voltage mode
Operating Mode Flag is cleared

Example PPS Responses

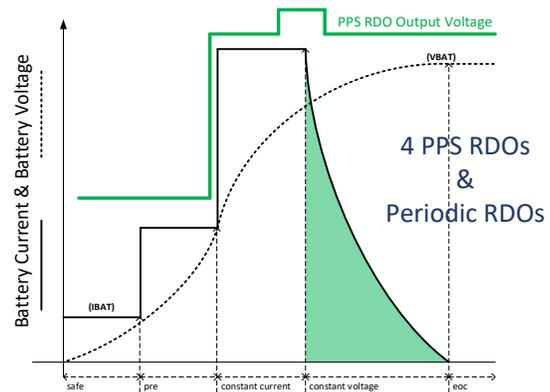
“The Presenter”



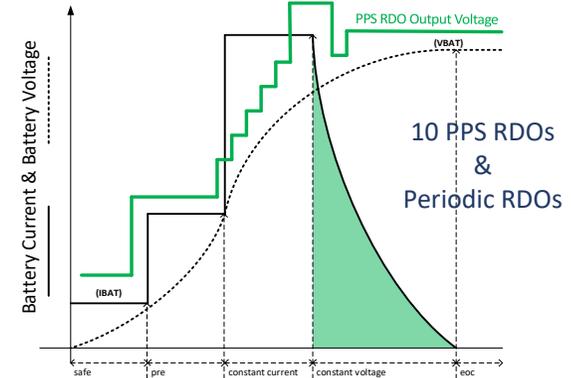
“The Cooler”



“The Nudge”



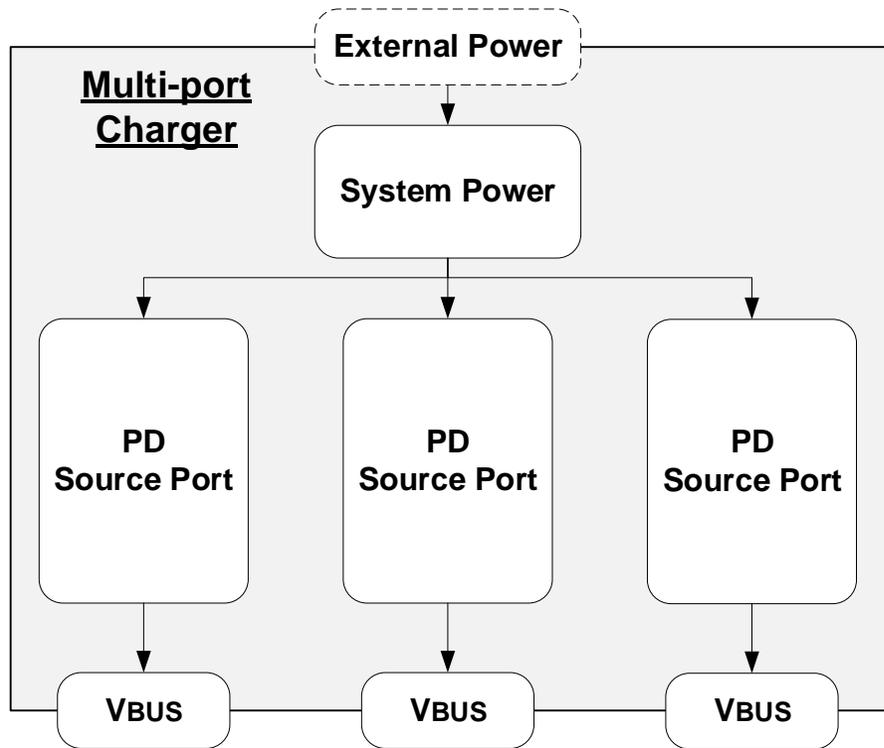
“The Optimizer”



Charging

- Overview
- Fixed Supply
- PPS
- **Multi-port**
- Good to know

Charger Configurations

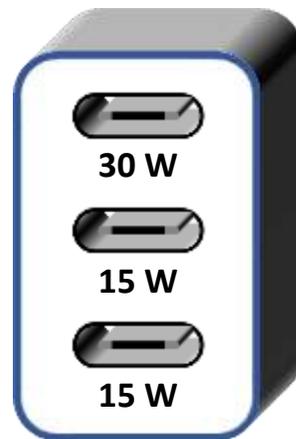


- Multi-port charger has more than one downstream charging port
- Assured Capacity Charger
 - Can supply full PDP on every port all of the time
 - One big supply or dedicated per port
- Shared Capacity Charger
 - Total PDP is shared between ports
 - Allocates power dynamically e.g.:
 - First come first served
 - Low ball + Capability Mismatch
 - Uses Sink Extended Capabilities to determine Sink Power needs
 - Min, operating max PDP

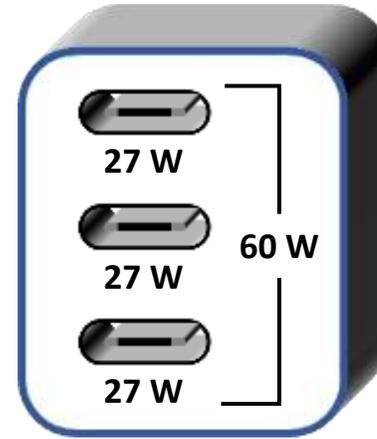
USB Type-C® Multi-Port Chargers – Port Identification

- Two categories of charger ports
 - Assured Capacity Ports
 - Each port is able to deliver its rated/labeled power capacity independent of all other ports
 - Shared Capacity Ports
 - Each port is able to deliver up to its rated/labeled power capacity depending on the remaining available capacity that is shared by a group of multiple ports
 - The total available power capacity of the group of ports is indicated to the user and all ports in the group are *capable* of delivering to the same power rating

Example of an Assured Capacity Charger that has a total capability of 60 W and a USB Charger certification of 30 W



Example of a Shared Capacity Charger that has a total capability of 60 W and a USB Charger certification of 27 W



Charging

- Overview
- Fixed Supply
- PPS
- Multi-port
- **Good to know**

PPS – *What can go wrong?*

- Output voltage did not increment/decrement from previous value
 - Output is supposed to be monotonic with 20 mV steps
- Output voltage transition times not met on large voltage changes
- Current Limit mode not supported
 - Required for PPS
- Minimum voltage
 - 3.3 V requirement not met
- PPS Status
 - OMF flag not properly set
 - Voltage/Current not reported correctly
- Response to Hard Reset
 - Vbus discharge to vSafe0V
 - Active discharge or allow to decay – inconsistent behavior

Time for Q&A

Session Break

Agenda

- Introduction
- Charging
- **USB4™**
- Compliance

USB4™ Discovery and Entry Process

1. CC Connection State Machines resolve Source/Sink and initial data roles (DFP/UFP)
2. Initial VBUS and VCONN power is supplied
3. USB PD is used to establish a power contract between the port partners

These steps are common to all USB connections

4. USB PD **Discover Identity** is used by the DFP to identify port partner (SOP) capabilities
5. USB PD **Discover Identity** is used by the DFP to identify cable (SOP') capabilities
6. If the cable and port partner both support USB4 operation, the DFP issues USB PD **Enter_USB** messages to both the cable and port partner to enter USB4 operation

7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can optionally initiate a data-role swap in order to exchange host (master) and device (slave) roles

USB4™

- **Discover Identity**
- Enter USB
- Data Reset

Discover Identity

Header No. of Data Objects = 4-7 ¹	VDM Header	ID Header VDO	Cert Stat VDO	Product VDO	0..3 ² Product Type VDO(s)
--	------------	---------------	---------------	-------------	---------------------------------------

- Existing mechanism for discovering information related to PD devices and cables
- Uses Vendor Defined Command/Response
- Contains up to 3 Product Type VDOs with product specific information
- Extended existing Passive and Active Cable Product Type VDOs to include USB4™
- Added Product Type VDOs for DFP and UFP with USB4 related information

Passive Cable VDO

- Minimum change to add USB4™ support
- Gen2 is the same for USB 3.2 and USB4
- Gen3 gets a new value
 - Was reserved so ignored by existing systems

Bit(s)	Field	Description
...		
B2...0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 011b...111b = Reserved, Shall Not be used

Active Cable VDO 1

- Minimum change to add USB4™ support
- Gen2 is the same for USB 3.2 and USB4

Bit(s)	Field	Description
...		
B23...21	VDO Version	Version Number of the VDO (not this specification Version): <ul style="list-style-type: none">• Version 1.3 = 011b
...		
B2...0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 011b...111b = Reserved, Shall Not be used

Active Cable VDO 2

- U3 power also applies to USB4™ CLd
- Cable Type field added
- USB4 Supported field added
- Gen3 gets a new value
 - Was reserved so ignored by existing systems

Bit(s)	Field	Description
• • •		
B14...12	U3/CLd Power	000b: >10mW 001b: 5-10mW 010b: 1-5mW 011b: 0.5-1mW 100b: 0.2-0.5mW 101b: 50-200µW 110b: <50µW 111b: Reserved, Shall Not be used
• • •		
B10...9	Cable Type	00b = Reserved, Shall Not be used 01b = Active Retimer 10b = Active Redriver 11b = Optically Isolated Active Cable
B8	USB4 Supported	0b = [USB4] supported 1b = [USB4] not supported
• • •		
B0	USB Signaling Gen	0b = Gen 1 1b = Gen 2 or higher

UFP VDO 1

- Read by Host/Hub DFP
- Supplied by Hub/Device UFP
- New VDO:
 - Version number for the pair of UFP VDOs
 - Device capability at each speed
 - Support for alternate modes
 - Highest USB Speed supported

Table 6-35 UFP VDO 1

Bit(s)	Field	Description										
B31...29	UFP VDO Version	Version Number of the VDO (not this specification Version): <ul style="list-style-type: none"> • Version 1.0 = 000b Values 001b...111b are Reserved and Shall Not be used										
B28	Reserved	Shall be set to zero.										
B27...24	Device Capability	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[USB 2.0] Device Capable</td> </tr> <tr> <td>1</td> <td>[USB 2.0] Device Capable (Billboard only)</td> </tr> <tr> <td>2</td> <td>[USB 3.2] Device Capable</td> </tr> <tr> <td>3</td> <td>[USB4] Device Capable</td> </tr> </tbody> </table>	Bit	Description	0	[USB 2.0] Device Capable	1	[USB 2.0] Device Capable (Billboard only)	2	[USB 3.2] Device Capable	3	[USB4] Device Capable
		Bit	Description									
		0	[USB 2.0] Device Capable									
		1	[USB 2.0] Device Capable (Billboard only)									
		2	[USB 3.2] Device Capable									
3	[USB4] Device Capable											
B23...6	Reserved	Shall be set to zero.										
B5...3	Alternate Modes	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Supports [TBT3] Alternate Mode</td> </tr> <tr> <td>1</td> <td>Supports Alternate Modes that reconfigure the signals on the [USB Type-C 2.0] connector – except for [TBT3].</td> </tr> <tr> <td>2</td> <td>Supports Alternate Modes that do not reconfigure the signals on the [USB Type-C 2.0] connector</td> </tr> </tbody> </table>	Bit	Description	0	Supports [TBT3] Alternate Mode	1	Supports Alternate Modes that reconfigure the signals on the [USB Type-C 2.0] connector – except for [TBT3].	2	Supports Alternate Modes that do not reconfigure the signals on the [USB Type-C 2.0] connector		
		Bit	Description									
		0	Supports [TBT3] Alternate Mode									
		1	Supports Alternate Modes that reconfigure the signals on the [USB Type-C 2.0] connector – except for [TBT3].									
2	Supports Alternate Modes that do not reconfigure the signals on the [USB Type-C 2.0] connector											
B2...0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/[USB4] Gen2 011b = [USB4] Gen3 100b...111b = Reserved, Shall Not be used										

UFP VDO 2

Table 6-36 UFP VDO 2

Bit(s)	Field	Description
B31...30	Reserved	Shall be set to zero.
B29...23	USB4 Min Power	Minimum power in watts required to function in [USB4] operation.
B22...16	USB4 Max Power	Power in watts required for full functionality excluding any power required for battery charging or for redistribution in [USB4] operation.
B15...14	Reserved	Shall be set to zero.
B13...7	USB3 Min Power	Minimum power in watts required to function in [USB 3.2] operation.
B6...0	USB3 Max Power	Power in watts required for full functionality excluding any power required for battery charging or for redistribution in [USB 3.2] operation.

- Second VDO
 - Max/Min power in Watts for USB4™ operation
 - Max/Min power in Watts for USB3.2 operation

DFP VDO

- Read by:
 - DRD operating as UFP
 - PD tester in multi-port tests
- Supplied by:
 - Host/Hub DFP
 - DRD operating as a DFP
- New VDO:
 - Version number for the DFP VDOs
 - Host capability at each speed
 - Port Number

Table 6-37 DFP VDO

Bit(s)	Field	Description								
B31...29	DFP VDO Version	Version Number of the VDO (not this specification Version): <ul style="list-style-type: none"> • Version 1.0 = 000b Values 001b...111b are Reserved and Shall Not be used								
B28...27	Reserved	Shall be set to zero.								
B26...24	Host Capability	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[USB 2.0] Host Capable</td> </tr> <tr> <td>1</td> <td>[USB 3.2] Host Capable</td> </tr> <tr> <td>2</td> <td>[USB4] Host Capable</td> </tr> </tbody> </table>	Bit	Description	0	[USB 2.0] Host Capable	1	[USB 3.2] Host Capable	2	[USB4] Host Capable
		Bit	Description							
		0	[USB 2.0] Host Capable							
		1	[USB 3.2] Host Capable							
2	[USB4] Host Capable									
B23...5	Reserved	Shall be set to zero.								
B4...0	Port Number	Unique port number to identify a specific port on a multi-port device.								

Discover Identity – What do Ports return?

DFP

Header Data Objects = 5	VDM Header	ID Header VDO	Cert Stat VDO	Product VDO	Product Type VDO(s)	
					DFP	

UFP

Header Data Objects = 6	VDM Header	ID Header VDO	Cert Stat VDO	Product VDO	Product Type VDO(s)	
					UFP1	UFP2

DRD – Dual Role Data

Header Data Objects = 7	VDM Header	ID Header VDO	Cert Stat VDO	Product VDO	Product Type VDO(s)		
					UFP1	UFP2	DFP

- Can operate as either a DFP (Host) or UFP (Device)
- Indicates a DFP and UFP Product Type in its ID Header VDO
- Returns UFP VDO 1, then UFP VDO 2, then the DFP VDO

USB4™

- Discover Identity
- **Enter USB**
- Data Reset

Enter USB

- Used to enter a specific USB mode operation:
 - Particularly USB4™
 - Can be used for USB 3.2 and USB 2.0
- Process to enter USB4 defined in the USB Type-C® Cable and Connectors specification
- Initiated by the DFP to direct the UFP and Cable Plugs to enter USB4
- Includes DFP and cable information for UFP use

Enter USB – Supplies Information

- Provides information on the DFP’s capabilities to the UFP
 - Allows a DRD, operating as a UFP, to decide on a Data Role Swap when directly connected
- Provides information on the attached cable
 - UFP does not have to query cable capabilities
- Provides information on the Host’s presence and Alternate Mode support
 - Forwarded to the Hub tree
- Host Present bit indicates whether a Hub tree is “headless” or not
 - When no Host is connected tree can be speculatively trained
 - When Host is connected, Host Present bit is set, and Hub tree is retrained if needed

Enter USB info

Bit(s)	Field	Description
B31	Reserved	Shall be set to zero.
B30...28	USB Mode ¹	000b: [USB 2.0] 001b: [USB 3.2] 010b: [USB4] 111b...011b: Reserved, Shall not be used
B27	Reserved	Shall be set to zero.
B26	USB4 DRD ²	0b: Not capable of operating as a [USB4] Device 1b: Capable of operating as a [USB4] Device
B25	USB3 DRD ²	0b: Not capable of operating as a [USB 3.2] Device 1b: Capable of operating as a [USB 3.2] Device
B24	Reserved	Shall be set to zero.
B23...21	Cable Speed ²	000b: [USB 2.0] only, no SuperSpeed support 001b: [USB 3.2] Gen1 010b: [USB 3.2] Gen2 and [USB4] Gen2 011b: [USB4] Gen3 111b...100b: Reserved, Shall not be used
B20...19	Cable Type ²	00b: Passive 01b: Active Re-timer 10b: Active Re-driver 11b: Optically Isolated
B18...17	Cable Current ²	00b = VBUS is not supported 01b = Reserved 10b = 3A 11b = 5A
B16	PCIe Support ²	[USB4] PCIe tunneling supported by the host
B15	DP Support ²	[USB4] DP tunneling supported by the host
B14	TBT Support ²	[TBT3] is supported by the host's USB4 Connection Manager
B13	Host Present ²	Connected to a Host. When this bit is set PCIe Support, DP Support, and TBT Support represent the Host's capabilities that Shall be propagated down the Hub tree.
B12...0	Reserved	Shall be set to zero.
Note 1: Entry into [USB 3.2] and [USB4] include entry into [USB 2.0].		
Note 2: Shall be Ignored when received by a Cable Plug (e.g., SOP' or SOP'').		

USB4™

- Discover Identity
- Enter USB
- **Data Reset**

Effect of Data Reset

1. CC Connection State Machines resolve Source/Sink and initial data roles (DFP/UFP)
 2. Initial VBUS and VCONN power is supplied
 3. USB PD is used to establish a power contract between the port partners
 4. USB PD **Discover Identity** is used by the DFP to identify port partner (SOP) capabilities
 5. USB PD **Discover Identity** is used by the DFP to identify cable (SOP') capabilities
 6. If the cable and port partner both support USB4 operation, the DFP issues USB PD **Enter_USB** messages to both the cable and port partner to enter USB4 operation
-
7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can optionally initiate a data-role swap in order to exchange host (master) and device (slave) roles

Data Reset

Data Reset

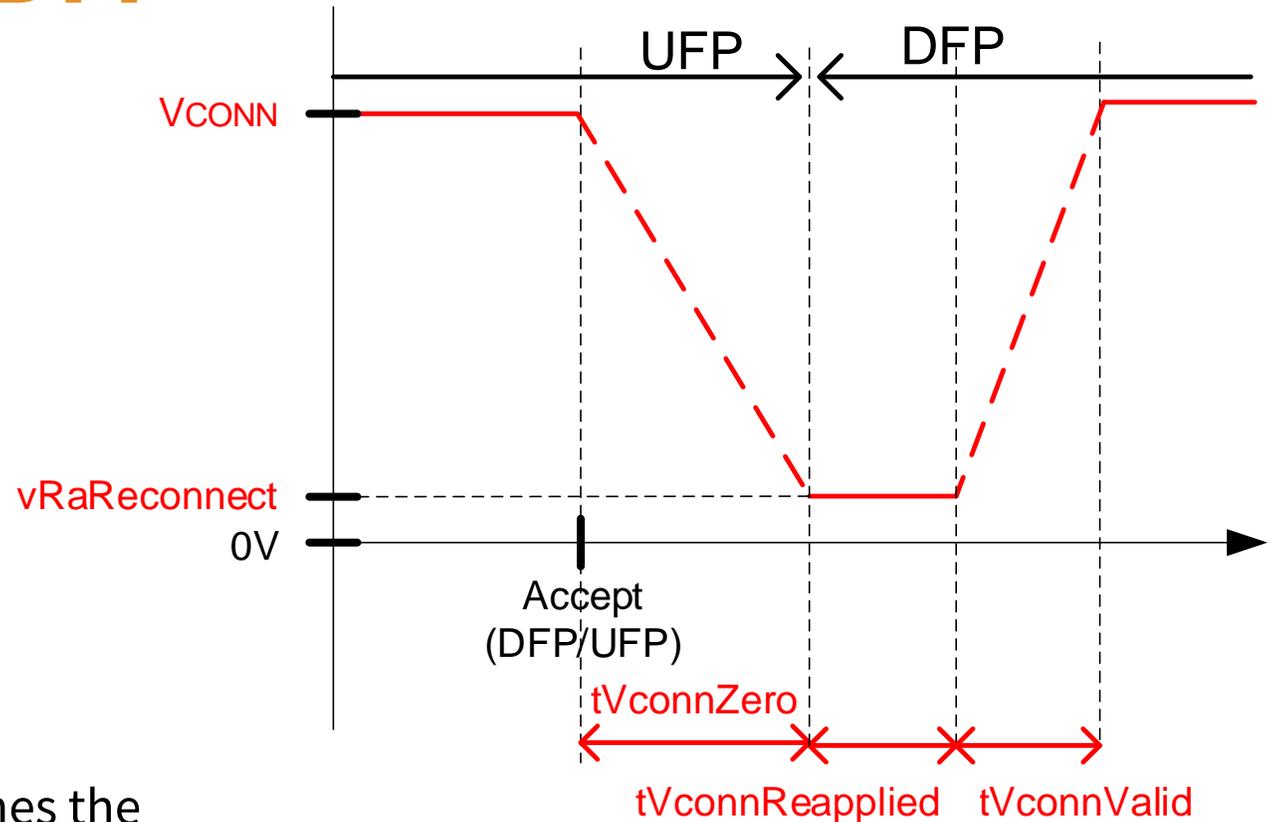
- Used to reset the USB data connection
- Sent by either the DFP or UFP
- Preserves power Contract, power and data roles
- Exits all active Alternate Modes
- Resets the cable by power cycling VCONN
- VCONN source reverts to the DFP and VCONN is turned on
- When Data Reset fails, ErrorRecovery (detach and reattach) is triggered

Data Reset Process

- DFP electrically disconnects the USB signaling:
 - Disconnects the Port's USB 2.0 D+/D- signals.
 - If operating in USB 3.2 the port's Rx Terminations are removed
 - If operating in USB4™ the port's SBTX is driven low
- Both the DFP and UFP exit all Alternate Modes if any
- Cable is reset by cycling VCONN
- DFP finishes the process as the VCONN Source and is supplying VCONN
- DFP electrically reconnects the USB signaling:
 - Reconnect the USB 2.0 D+/D- signals
 - If the Port was operating in USB 3.2 or USB4 the port's Rx Terminations are re-applied
- DFP sends Data_Reset_Complete message to the UFP
- The Data Reset process is complete

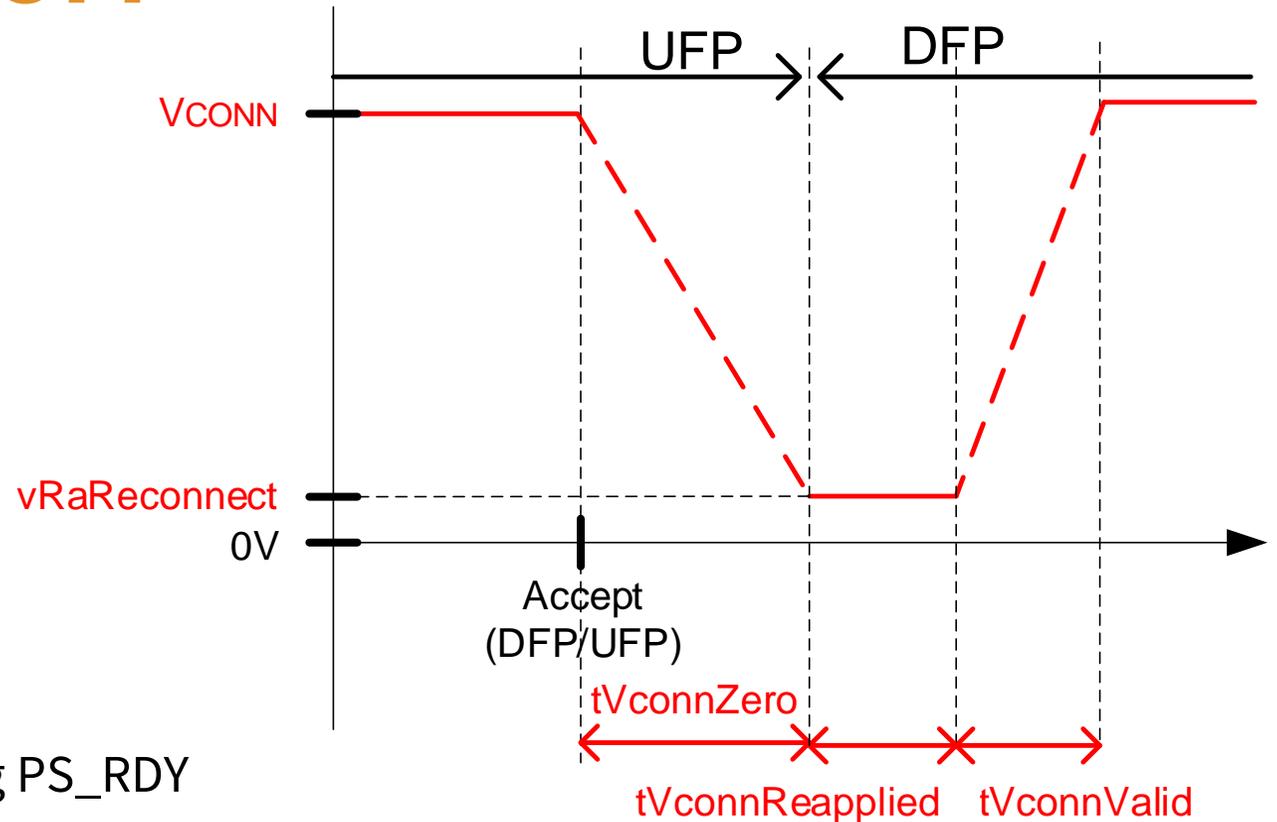
VCONN Power Cycle – DFP

- If the DFP is the VCONN Source and supplying VCONN
 - Turns off VCONN
 - VCONN drops below $v_{RaReconnect}$ within $t_{VconnZero}$
- In every case the DFP:
 - Waits $t_{VconnReapplied}$ after VCONN has dropped
 - Allows cable the time to perform a power cycle reset
 - After $t_{VconnReapplied}$ the DFP becomes the VCONN source and turns on VCONN
 - VCONN reaches $v_{VconnValid}$ (3 V – 5.5 V) within $t_{VconnValid}$



VCONN Power Cycle – UFP

- If the UFP is the VCONN Source and supplying VCONN
 - Turns off VCONN
 - VCONN drops below $v_{RaReconnect}$ within $t_{VconnZero}$
- In every case the UFP:
 - Sends PS_RDY to indicate that VCONN is off
- DFP:
 - Waits $t_{VconnReapplied}$ after receiving PS_RDY
 - Allows cable the time to perform a power cycle reset
 - After $t_{VconnReapplied}$ the DFP becomes the VCONN source and turns on VCONN
 - VCONN reaches $v_{VconnValid}$ (3 V – 5.5 V) within $t_{VconnValid}$



Time for Q&A

Agenda

- Introduction
- Charging
- USB4™
- **Compliance**

Compliance

- **Overview**
- Testing Issues
- Multi-port coming

General requirements

- Support of both PD2 and PD3 is still required
- Understand the specific procedures for selecting whether this connection speaks PD2 or PD3 and when it may change
- Precedence rules
- Be sure to understand the USB Type-C[®] specification as well

New PD3 Compliance Specification

- Originally there were three specs
 - Two for PD2 and one for PD3
 - Compliant device must pass all three
- New PD3 Compliance spec
 - Combines three existing specs into a single document
 - Single approach for all tests required for PD3 device
 - Adds requirement to run certain tests in both PD2 and PD3 modes
 - Specifies how the Tester shall respond to all UUT initiated messages, regardless of whether they are part of the normal test steps
- Initial release
 - Released September 2019
 - Does not include FRS tests

New PD3 Compliance summary

- The Test Specification has two main parts
 - Common Procedures and Checks
 - Test Procedures
- The Tester runs the Common Procedures and Checks for all applicable procedures and checks
 - The applicability of Common Check for a given PD message is provided in Check Applicability
 - The applicability of Common Procedure is provided in Procedure Applicability
- The Tester runs all Test Procedures applicable to the UUT
 - The UUT applicability is determined by the VIF fields and it is provided at the beginning of each subsection

Compliance

- Overview
- **Testing Issues**
- Multi-port coming

Following the spec is important

- Simple things can cause big problems
- Reserved bits / values
 - Spec requirement: Set to 0 by the sender – *to be ignored by the receiver*
 - Rationale was to allow these bits to be used by future revisions without impacting previous revisions
- Problem seen in the field
 - Revision 3 APDO used for PPS defined a previously reserved value
 - Some Revision 3 Sinks did not ignore the reserved value and could not properly understand the new data object and did Hard Resets
 - The result is that they would not get any power from a properly operating PPS charger – *Bad User Experience!*

VCONN Source

- Being a VCONN Source means that this Port is the only one allowed to **actually source** VCONN at the time
- Sourcing VCONN (actually applying the voltage) is done at the discretion of the VCONN Source Port
- Listening on SOP', SOP'' is **only** allowed for the Port that is currently the VCONN Source
 - Otherwise both the remote port and the cable will send GoodCRC at the same time

Pay Special Attention

- Chapter 7
 - 7.3 Transitions there are some important timing things here.
- Chapter 8
 - Study both the *Atomic Message Sequence Diagrams* and the *State Diagrams*

Physical Layer

- Be careful with the transmitter eye – *keep a safe distance to the masks*
- Receiver
 - Bit-rate is $\pm 10\%$, will be tested
 - Interference rejection will be tested
 - Look at noise specifications
 - Be aware that there is an offset of 250 mV in some cases – *this is the big killer*
- Note that the Rp is used for collision avoidance in PD3 but not in PD2
 - There are timing requirements that will be tested

GoodCRC Message

- The GoodCRC Message has only one meaning:
 - The message sent has arrived intact with all its bits and they are all correct
 - There is ***no other meaning*** in this message
- The time allowed for the transmission of the GoodCRC Message is critical, 25 μ s – 195 μ s
- It is not allowed to fail to reply with a GoodCRC message in order to gain time to finish SW tasks
 - This will be tested and will result in a failure in compliance.
 - Retries are meant for combating noise and can not be used to compensate for slow SW

PPS testing issues fixed by vendors

- CL Mode in general not implemented correctly or not working with our particular simulated CR load
- Not setting OMF flag in CL mode
- CV Mode voltage 20 mV steps not always stepping (big jump and then no jumps for a while)
- CV Mode voltage tuned a little high or low and needs tweak and retest to stay in vPpsNew range
- CL Mode current tuned a little high or low and needs tweak and retest to stay in iPpsCLNew range
- Big voltage transitions on (> 500 mV) RDO request changes

PPS testing issues fixed in the spec

- iPpsCLOperating failure to stay within 10 mV tolerance
 - This one was a big issue for which a larger tolerance and linear requirement was introduced in the base spec
- Power Limited bit implementation was based on RDO request instead of actual power draw
 - Spec updated to clarify that RDO request was the way to limit power instead of actual power draw

PPS testing issues still seen

- Transient voltage overshoot
- OMF flag setting slightly late / early
- iPpsCLOperating failure to stay within 25 mV / linear tolerance
- Thermal shutdown during testing
 - Devices thermally shutdown during the 1 – 2 hour test cycle under normal (non-OC) conditions

Test Team Feedback

- *The good news is that testing is working and most implementations are passing!*
 - We've noticed a *drastic* improvement over time of vendor PPS implementations
 - At the start it wasn't even clear that people knew that a CL mode had to be implemented
 - There were *so many 1000s of failures* that we had to make an additional csv output to collate and parse all of them and it took hours to analyze & explain results
 - Now we hardly use that csv file because vendors aren't failing as spectacularly

Compliance

- Overview
- Testing Issues
- **Multi-port coming**

Multi-port Compliance is coming

- Single port charger compliance testing is well in place – expansion to multiple port is challenging
- PD additions to facilitate multi-port charger testing
 - Port identification using the discover ID
 - Test mode for testing shared
- Test equipment
 - Existing test equipment (QuadraMax) can only test assured sources with fixed outputs
 - New test equipment needed to test shared sources and PPS
- Multi-port spec is in draft stage
 - Testing will be phased in starting with assured sources with fixed outputs
 - Testing of shared sources and PPS will follow as test equipment is developed

Time for Q&A
