DisplayPort™ CTS Tool Options for UCD-500 Gen2

Guide to Product Options

UNIGRAF

Copyright

Notice

The information given in this manual is verified in the correctness on the date of issue. The authors reserve the rights to make any changes to this product and to revise the information about the products contained in this manual without an obligation to notify any persons about such revisions or changes.

Edition

DisplayPort CTS Tools for UCD-500 Gen2, rev 10

Date: 12 December 2025

Company information

Unigraf
Piispantilankuja 4, FI-02240 ESPOO, Finland

info@unigraf.fi

https://www.unigraf.fi

http://www.unigraf-china.cn

Table of Content

1. GENERAL

DP 2.1 Reference Hardware Products

Product	P/N	Description
UCD-500 Gen2	066710	DP 2.1 capable test unit for DisplayPort Sink and Source up to 10K@60Hz 24bpp. Support DP and USB-C connectors. USB 3.0 Interface to Host PC.

DP Link CTS Test Software Product Options

Product	P/N	Description
DP 1.4a LL CTS for testing Source DUT	MT6637	DP 1.4a LL, FEC & Audio compliance tests for testing Source DUT.
DP 1.4a LL CTS for testing Sink DUT	MT6635	DP 1.4a LL, FEC & Audio compliance tests for testing Sink DUT.
DP 2.1 LL CTS for testing Source DUT	MT6662	DP 2.1 LL compliance tests for testing Source DUT. Audio, DSC and FEC CTS included.
DP 2.1 LL CTS for testing Sink DUT	MT6660	DP 2.1 LL compliance tests for testing Sink DUT. Audio, DSC and FEC CTS included.
DP 2.1 + DP 1.4a LL CTS for testing Source DUT	MT6662 + MT6637	DP 1.4a & DP 2.1 LL compliance tests for testing Source DUT. Audio, DSC and FEC CTS included.
DP 2.1 + DP 1.4a LL CTS for testing Sink DUT	MT6660 + MT6635	DP 1.4a & DP 2.1 LL compliance tests for testing Sink DUT. Audio, DSC and FEC CTS included.
DP 1.4a DSC CTS for testing Source DUT	MT6642	Display Stream Compression compliance tests for testing Source DUT.
DP 1.4a DSC CTS for testing Sink DUT	MT6643	Display Stream Compression compliance tests for testing Sink DUT.
DP 2.1 DSC CTS for testing Source DUT	MT6656	Display Stream Compression compliance tests for testing Source DUT. (*
DP 2.1 DSC CTS for testing Sink DUT	MT6657	Display Stream Compression compliance tests for testing Source DUT. (*
DP 2.1 + DP 1.4a DSC CTS for testing Source DUT	MT6656 + MT6642	Combine for testing DP 2.1 / 1.4a DSC CTS Source DUT. (*
DP 2.1 + DP 1.4a DSC CTS for testing Sink DUT	MT6657 + MT6643	Combine for testing DP 2.1 / 1.4a DSC CTS Sink DUT. (*
DP 2.1 DisplayID/EDID CTS for testing Source DUT	MT6646	DisplayID CTS for testing Source DUT.
DP 2.1 DisplayID/EDID CTS for testing Sink DUT	MT6647	DisplayID CTS for testing Sink DUT.
DP 2.1 Adaptive-Sync CTS for testing Source DUT	MT6648	Adaptive-Sync CTS for testing Source DUT.
DP 2.1 Adaptive-Sync CTS for testing Sink DUT	MT6649	Adaptive-Sync CTS for testing Sink DUT.
DP 2.1 LTTPR CTS for testing Source DUT	MT6680	LTTPR CTS (tests 4.9.x) for testing Source DUT.
DP 2.1 LTTPR CTS for testing Sink DUT	MT6679	LTTPR CTS (tests 5.9.x) for testing Sink DUT.
DP 2.1 LTTPR CTS for testing LTTPR DUT	MT6681	LTTPR compliance test for testing LTTPR Device. (*

Test Software Content

Source DUT Testing		DP 1.4a LL CTS*	DP 1.4a DSC CTS*	DP 2.1 LL CTS*	DP 2.1 DSC CTS*	DisplayID/EDID CTS*	Adaptive-Sync CTS*	DP 2.1 LTTPR CTS*
DP 1.4a Link Layer CTS	• 4.2.1.1 – 4.2.1.5 • 4.2.2.1 – 4.2.2.10 • 4.3.1.1 – 4.3.1.13 • 4.3.2.1 – 4.3.2.5 • 4.3.3.1 • 4.4.1.1 – 4.4.1.3 • 4.4.2, 4.4.3 • 4.4.4.2 – 4.4.4.6 • 4.5.1.1 – 4.5.1.2	●						
DP 1.4a DSC CTS	• 4.6.1.1 – 4.6.1.9		●					
DP 2.1 Link Layer CTS	• 4.2.1.1 – 4.2.1.5 • 4.2.2.1 – 4.2.2.2 • 4.2.2.4 – 4.2.2.5 • 4.2.2.7 – 4.2.2.8 • 4.2.2.10 – 4.2.2.14 • 4.3.1.1 – 4.3.1.24 • 4.3.2.1 – 4.3.2.4 • 4.3.3.1 – 4.3.3.2 • 4.4.1.1 - 4.4.1.6 • 4.4.2.1 – 4.4.2.2 • 4.4.3 • 4.4.4.2 – 4.4.4.13 • 4.5.1.1 – 4.5.1.2			●				
DP 2.1 DSC CTS	• 4.6.1.1 – 4.6.1.9				●			
DP 2.1 DisplayID/EDID CTS**	• 4.7.1.1 – 4.7.1.4 • 4.7.2.1 – 4.7.2.2 • 4.7.3.1 – 4.7.3.3 • 4.7.4.1, 4.7.4.4 • 4.7.5.1 • 4.7.6.1 - 4.7.6.4 • 4.7.7.1 - 4.7.7.2					●		
DP 2.1 Adaptive-Sync LL CTS**	• 4.8.1.1 – 4.8.1.2 • 4.8.2.1 – 4.8.2.3						●	
DP 2.1 LTTPR CTS	• 4.9.1.1 – 4.9.1.22							●

*) Separate licenses for testing Sink, Source, Branch (LL CTS, DSC, DisplayID) DUT

**) Unigraf UCD-400 was used by VESA for TE correlation of the tests

Sink DUT Testing		DP 1.4a LL CTS*	DP 1.4a DSC CTS*	DP 2.1 LL CTS*	DP 2.1 DSC CTS*	DisplayID/EDID CTS*	Adaptive-Sync CTS*	DP 2.1 LTTPR CTS*
DP 1.4a Link Layer CTS	• 5.2.1.1 – 5.2.1.12 • 5.2.2.1 – 5.2.2.9 • 5.3.1.1 – 5.3.1.9 • 5.3.2.1 – 5.3.2.2 • 5.4.1.1 – 5.4.1.4 • 5.4.2, 5.4.3.1 – 5.4.3.2 • 5.4.4.1 – 5.4.4.6 • 5.5.1.1 – 5.5.1.7	●						
DP 1.4a DSC CTS	• 5.6.1.1 – 5.6.1.26 • 5.6.2.1 – 5.6.2.14		●					
DP 2.1 Link Layer CTS	• 5.2.1.8 – 5.2.1.12 • 5.2.2.1 – 5.2.2.3 • 5.2.2.5 – 5.2.2.10 • 5.3.1.1 – 5.3.1.5 • 5.3.1.8 – 5.3.1.15 • 5.3.2.1 – 5.3.2.2 • 5.4.1.1 – 5.4.1.8 • 5.4.2.1 – 5.4.2.2 • 5.4.3.1 - 5.4.3.4 • 5.4.4.1 - 5.4.4.10 • 5.4.5.1 - 5.4.5.5 • 5.5.1.1 - 5.5.1.12			●				
DP 2.1 DSC CTS	• 5.6.1.1 – 5.6.1.26 • 5.6.2.1 – 5.6.2.16 • 5.6.3.1 – 5.6.3.7				●			
DisplayID/EDID CTS**	• 5.7.1.1 – 5.7.1.2 • 5.7.1.3.1 – 5.7.1.3.4 • 5.7.1.4.1 – 5.7.1.4.9 • 5.7.1.5 – 5.7.1.6 • 5.7.2.1 – 5.7.2.2 • 5.7.2.3.1 – 5.7.2.3.5 • 5.7.2.4.1 – 5.7.2.4.2 • 5.7.2.5.1 – 5.7.2.5.2 • 5.7.2.6.1 – 5.7.2.6.2 • 5.7.2.7.1 • 5.7.2.8 • 5.7.3.1 – 5.7.3.5 • 5.7.4.1 – 5.7.4.3 • 5.7.4.5 • 5.7.5.1 • 5.7.6.1 – 5.7.6.5 • 5.7.7.1 – 5.7.7.6 • 5.7.8.1 – 5.7.8.6 • 5.7.9.1 – 5.7.9.3					●		

	• 5.7.10.1 – 5.7.10.3 • 5.7.11.1 – 5.7.11.5 • 5.7.12.1 – 5.7.12.4 • 5.7.13.1 – 5.7.13.2 • 5.7.14.1 – 5.7.14.8 • 5.7.15.1 – 5.7.15.11 • 5.7.16.1 – 5.7.16.7 • 5.7.16.9 – 5.7.16.10 • 5.7.17.1 – 5.7.17.5 • 5.7.18.1 • 5.7.19.1 - 5.7.19.6 • 5.7.20.1 - 5.7.20.3 • 5.7.21.1 - 5.7.21.5 • 5.7.22.1 - 5.7.22.7							
Adaptive-Sync LL CTS**	• 5.8.1.1 – 5.8.1.3						●	
DP 2.1 LTTPR CTS	• 5.9.1.1 – 5.9.1.15							●

*) Separate licenses for testing Sink, Source, Branch (LL CTS, DSC, DisplayID) DUT

LTTPR DUT Testing		DP 2.1 LTTPR CTS for testing LTTPR Device
DP 2.1 LTTPR CTS for testing LTTPR DUT	• 7.1.1.1 – 7.1.1.9 • 7.1.2.1 – 7.1.2.9 • 7.1.3.1-7.1.3.8 • 7.1.4.1-7.1.4.10 • 7.1.5.1-7.1.5.6 • 7.1.6.1-7.1.6.7 • 7.1.7.1-7.1.7.7 • 7.1.8.1 • 7.1.9.1 • 7.1.10.1 - 7.1.10.2 • 7.1.11.1 - 7.1.11.2 • 7.1.12.1 - 7.1.12.8	●

2. LINK CTS FOR TESTING SOURCE DUT

DP 1.4a LL CTS for testing Source DUT (P/N: MT6637)

AUX Reads after HPD Plug Event

Test Reference	Test Name
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event
4.2.1.3	Source Device HPD Event Pulse Length Test
4.2.1.4	Source Device IRQ_HPD Pulse Length Test
4.2.1.5	Source Device Inactive HPD / Inactive AUX Test

EDID and DPCD Reads

Test Reference	Test Name
4.2.2.1	DPCD Receiver Capability and EDID Read upon HPD Plug Event
4.2.2.2	DPCD Receiver Capability Read upon HPD Plug Event
4.2.2.3	EDID Read
4.2.2.4	EDID Read Failure #1: I2C-Over-AUX NACK
4.2.2.5	EDID Read Failure #2: I2C-Over-AUX DEFER
4.2.2.6	Source Device Inactive HPD / Inactive AUX test
4.2.2.7	Branch Device Detection upon HPD Plug Event
4.2.2.8	EDID Read on IRQ HPD Event after Branch Device Detection
4.2.2.9	E-DDC Four Block EDID Read
4.2.2.10	Link Status-Adjust Request AUX read interval during Link Training

Link Training

Test Reference	Test Name
4.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds
4.3.1.2	Successful Link Training Upon HPD Plug Event
4.3.1.3	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
4.3.1.4	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing
4.3.1.5	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing
4.3.1.6	Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence
4.3.1.7	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
4.3.1.8	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing
4.3.1.9	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing
4.3.1.10	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)
4.3.1.11	Successful LT with Simultaneous Request for Differential Voltage Swing and Pre-emphasis during Clock Recovery Sequence
4.3.1.12	Source Device Link Training CR Fallback Test
4.3.1.13	Source Device Link Training EQ Fallback Test

Link Maintenance

Test Reference	Test Name
4.3.2.1	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock
4.3.2.2	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock
4.3.2.3	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock
4.3.2.4	Handling of IRQ HPD Pulse with No Error Status Bits Set
4.3.2.5	Lane Count Reduction

Video Time Stamp Generation

Test Reference	Test Name
4.3.3.1	Video Time Stamp Generation

Main Stream Data Mapping

Test Reference	Test Name
4.4.1.1	Pixel Data Packing and Steering
4.4.1.2	Main Stream Data Packing and Stuffing – Least Packed TU
4.4.1.3	Main Stream Data Packing and Stuffing – Most Packed TU

4.4.2	Main Video Stream Format Change Handling

4.4.3	Power Management

Audio Stream Transmission over Secondary Packets

Test Reference	Test Name
4.4.4.2	Audio Stream Header Synchronization
4.4.4.3	Audio Time Stamp Generation
4.4.4.4	Audio InfoFrame Packet
4.4.4.6	Audio Start Sequence

Source FEC Protocol

Test Reference	Test Name
4.5.1.1	FEC enable verification for all supported Lane count and Link Speed
4.5.1.2	FEC ready verification for non FEC capable sink

DP DSC 1.4a CTS for testing Sink DUT (P/N MT6642)

Source Device DSC Test Procedures

Test Reference	Test Name
4.6.1.1	DSC enable sequence verification
4.6.1.2	DSC PPS block prediction flag verification
4.6.1.3	DSC PPS convert RGB flag verification
4.6.1.4	DSC PPS YCbCr 4:4:4 convert RGB = 0) flag verification
4.6.1.5	DSC PPS Simple 4:2:2 flag verification
4.6.1.6	DSC PPS Native 4:2:2 flag verification
4.6.1.7	DSC PPS Native 4:2:0 flag verification
4.6.1.8	DSC PPS convert RGB flag verification for DSC Algorithm Revision 1.1
4.6.1.9	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm Revision 1.1

DP 2.1 LL CTS for testing Source DUT (P/N: MT6662)

AUX Reads after HPD Plug Event

Test Reference	Test Name
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event
4.2.1.3	Source Device HPD Event Pulse Length Test
4.2.1.4	Source Device IRQ_HPD Pulse Length Test
4.2.1.5	Source Device Inactive HPD / Inactive AUX Test

EDID and DPCD Reads

Test Reference	Test Name
4.2.2.1	DPCD Receiver Capability and EDID Read upon HPD Plug Event
4.2.2.2	DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event
4.2.2.4	EDID Read Failure #1: I2C-Over-AUX NACK
4.2.2.5	EDID Read Failure #2: I2C-Over-AUX DEFER
4.2.2.7	Branch Device Detection upon HPD Plug Event
4.2.2.8	EDID Read on IRQ HPD Event after Branch Device Detection
4.2.2.10	Link Status/Adjust Request AUX read interval during Link Training
4.2.2.11	Various UHBR AUX read interval verification in first EQ loop
4.2.2.12	UHBR Link Status/Adjust different FFE Request, different AUX read interval for 10 EQ loop
4.2.2.13	Native AUX defer retry validation for Source DUT before link training
4.2.2.14	Native AUX defer retry validation for Source DUT during link training just after TPS1

Link Training

Test Reference	Test Name
4.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds
4.3.1.2	Successful Link Training Upon HPD Plug Event
4.3.1.3	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
4.3.1.4	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing

4.3.1.5	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing
4.3.1.6	Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence
4.3.1.7	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
4.3.1.8	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing
4.3.1.9	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing
4.3.1.10	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)
4.3.1.11	Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & Channel Equalization Sequences
4.3.1.12	Source Device Link Training CR Fallback Test
4.3.1.13	Source Device Link Training EQ Fallback Test

4.3.1.14	Successful Link Training at All Supported Lane Counts and UHBR Link Speeds
4.3.1.15	Successful Link Training Upon HPD Plug Event for UHBR speed.
4.3.1.16	Successful Link Training when EQ done at 20th loop during channel EQ phase
4.3.1.17	Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bits not set in 20 loops during channel EQ phase
4.3.1.18	Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random value 1 to 19)* during channel EQ Done
4.3.1.19	Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done
4.3.1.20	Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done
4.3.1.21	Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_DONE bit not set during EQ phase
4.3.1.22	Successful Link Training to a Lower Bandwidth. When Symbols not locked during CDS phase.
4.3.1.23	Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALIGN_DONE bit not set during CDS phase.
4.3.1.24	UHBR Fallback rate table validation

Link Maintenance

Test Reference	Test Name
4.3.2.1	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock
4.3.2.2	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock
4.3.2.3	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock
4.3.2.4	Handling of IRQ HPD Pulse with No Error Status Bits Set

Video Time Stamp Generation

Test Reference	Test Name
4.3.3.1	8b10b Rate Video Time Stamp Generation
4.3.3.2	UHBR Video Time Stamp Generation

Main Stream Data Mapping

Test Reference	Test Name
4.4.1.1	8b10b Rate Pixel Data Packing and Steering
4.4.1.2	8b10b Rate Main Stream Data Packing and Stuffing Least Packed TU
4.4.1.3	8b10b Rate Main Stream Data Packing and Stuffing Most Packed TU
4.4.1.4	UHBR Rate Pixel Data Packing and Steering
4.4.1.5	UHBR Rate Main Stream Data Packing and Stuffing Least Packed MTP
4.4.1.6	UHBR Rate Main Stream Data Packing and Stuffing Most Packed MTP

Main Video Stream Format Change Handling

Test Reference	Test Name
4.4.2.1	8b10b Rate Main Video Stream Format Change Handling
4.4.2.2	UHBR Rate Main Video Stream Format Change Handling
4.4.3	Power Management

Audio Stream Transmission over Secondary Packets

Test Reference	Test Name
4.4.4.2	Audio Stream Header Synchronization
4.4.4.3	Audio Time Stamp Generation
4.4.4.4	Audio InfoFrame Packet
4.4.4.5	Audio Stream Transmission
4.4.4.6	Audio Start Sequence
4.4.4.7	DSC (RB2 Timing) Audio Stream Transmission
4.4.4.8	UHBR Audio Stream Header Synchronization
4.4.4.9	UHBR Audio Time Stamp Generation
4.4.4.10	UHBR Audio InfoFrame Packet
4.4.4.11	UHBR Audio Stream Transmission
4.4.4.12	UHBR Audio Start Sequence
4.4.4.13	UHBR DSC (RB2 Timing) Audio Stream Transmission

Source FEC Protocol

Test Reference	Test Name
4.5.1.1	8b10b Rate Main Video Stream Format Change Handling
4.5.1.2	UHBR Rate Main Video Stream Format Change Handling

DP 2.1 DSC CTS for testing Source DUT (P/N: MT6656)

Source Device DSC Test Procedures

Test Reference	Test Name
4.6.1.1	DSC enable sequence verification
4.6.1.2	DSC PPS block prediction flag verification
4.6.1.3	DSC PPS convert RGB flag verification
4.6.1.4	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification
4.6.1.5	DSC PPS Simple 4:2:2 flag verification
4.6.1.6	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm Revision 1.1
4.6.1.7	DSC PPS Native 4:2:0 flag verification
4.6.1.8	DSC PPS convert RGB flag verification for DSC Algorithm Revision 1.1
4.6.1.9	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm Revision 1.1

DisplayID/EDID CTS for testing Source DUT (P/N: MT6646)

Note: Unigraf UCD-400 was used by VESA for TE correlation of the tests

Video Tests

Test Reference	Test Name
4.7.1.1	Basic Supported Formats
4.7.1.2	Preferred Timing
4.7.1.3	Out-of-Range Request
4.7.1.4	Invalid EDID

Audio Tests

Test Reference	Test Name
4.7.2.1	Basic Supported Formats
4.7.2.2	Out-of-Range Request

Source Device Test Procedures (E-DDC Protocol)

Test Reference	Test Name
4.7.3.1	EDID Read with More than 256 Bytes of Data Including DisplayID Block
4.7.3.2	EDID Read with Greater than 8 Blocks of Data Including DisplayID Block
4.7.3.3	EDID Read with Unknown Extensions and Unknown Data Blocks, Including DisplayID Block

Source Device Test Procedures (DisplayID)

Test Reference	Test Name
4.7.4.1	DisplayID Detailed Timing support
4.7.4.4	Dynamic Refresh Rate with Vertical Blank Stretch with MSA_TIMING_PAR_IGNORED

Source Device Test Procedures (Adaptive-Sync)

Test Reference	Test Name
4.7.5.1	DisplayID Adaptive-Sync CVT RB Timing v3 Support

Source Device Test Procedures (Native DisplayID Video Tests)

Test Reference	Test Name
4.7.6.1	Basic Supported Formats
4.7.6.2	Preferred Timing
4.7.6.3	Out-of-Range Request
4.7.6.4	Invalid DisplayID Structure

Source Device Test Procedures (Native DisplayID Audio Tests)

Test Reference	Test Name
4.7.7.1	Basic Supported Formats
4.7.7.2	Out-of-Range Request

Adaptive-Sync CTS for testing Source DUT (P/N: MT6648)

Note: Unigraf UCD-400 was used by VESA for TE correlation of the tests

Fixed-Average VTotal Mode Support Validation

Test Reference	Test Name
4.8.1.1	EDID - Fixed-Average VTotal Mode Support over the Declared Frame Rate Range
4.8.1.2	EDID - Fixed-Average VTotal Mode Duration Increase and Decrease Constraint Value Support

Adaptive VTotal Mode Support Validation

Test Reference	Test Name
4.8.2.1	EDID - Adaptive VTotal Mode Support with Duration Increase and Decrease Constraint Values
4.8.2.2	EDID - Adaptive VTotal Mode Support with Unconstrained Duration Increase and Decrease
4.8.2.3	EDID – Adaptive VTotal Mode Support in Gaming Environment

LTTPR CTS For Testing Source DUT (P/N: MT6680)

Source Embedded LTTPR protocol

Test Reference	Test Name
4.9.1.1	With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.2	With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.3	With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.4	With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.5	With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.6	With 6 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.7	With 7 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.8	With 8 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds
4.9.1.9	With random[1-8] number of emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds, Sink support 4 lane and all rates
4.9.1.10	With random[1-8] number of emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds, LTTPR support 4 lane and all rates
4.9.1.11	With random[1-8] number of emulated LTTPR, Successful Link Training (Higher Differential Voltage Swing during Clock Recovery)

4.9.1.12	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Link Rate/BW #1: Iterate at Maximum Voltage Swing
4.9.1.13	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Link Rate/BW #2: Iterate at Minimum Voltage Swing
4.9.1.14	With random[1-8] number of emulated LTTPR, Successful Link Training (HigherPre-emphasis Setting during Channel Equalization)
4.9.1.15	With random[1-8] number of emulated LTTPR, Successful Link Training (Lower Link Rate/BW During Channel Equalization)
4.9.1.16	With random[1-8] number of emulated LTTPR, Successful Link Training when EQ done at 20th loop during channel EQ phase
4.9.1.17	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bits not set in 20 loops during channel EQ phase
4.9.1.18	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random value 1 to 19) during channel EQ Done
4.9.1.19	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done
4.9.1.20	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done
4.9.1.21	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_DONE bit not set during EQ phase
4.9.1.22	With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When Symbols not locked during CDS phase

3. LINK CTS FOR TESTING SINK DUT

DP 1.4a LL CTS for testing Sink DUT (P/N MT6635)

AUX Channel Protocol

Test Reference	Test Name
5.2.1.1	Read One Byte from Valid DPCD Address
5.2.1.2	DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)
5.2.1.3	Write One Byte to Valid DPCD Address
5.2.1.4	Write Nine Bytes to Valid DPCD Addresses
5.2.1.5	Write EDID Offset (One Byte I2C-Over-AUX Write)
5.2.1.6	Read One EDID Byte (One Byte I2C-Over-AUX Read)
5.2.1.7	EDID Read (1 Byte I2C -Over-AUX Segment Write, 1 Byte I2C-Over-AUX Offset Write, 128 Byte I2C-Over-AUX Read)
5.2.1.8	Illegal AUX Request Syntax
5.2.1.9	Glitch Rejection
5.2.1.10	Interleaved EDID and DPCD Receiver Capability Read
5.2.1.11	Downstream Stop on MOT Reset
5.2.1.12	Downstream Stop on Timeout

Sink Device DPCD Field Implementation Addendum

Test Reference	Test Name
5.2.2.1	Sink Organizationally Unique Identifier (OUI)
5.2.2.2	Sink Count
5.2.2.3	Sink Status
5.2.2.4	Sink Error Count
5.2.2.5	DPCD Address Range
5.2.2.6	Number of Receiver Ports
5.2.2.7	Main Link Channel Coding
5.2.2.8	ESI Field Mapping
5.2.2.9	Sink Device Symbol Error Count

Link Training

Test Reference	Test Name
5.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds
5.3.1.2	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
5.3.1.3	Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure During Clock Recovery Sequence
5.3.1.4	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence
5.3.1.5	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
5.3.1.6	Lane Count Reduction
5.3.1.7	Lane Count Increase
5.3.1.8	2-Lane Link Training CR/EQ Fallback Test
5.3.1.9	1-Lane Link Training CR/EQ Fallback Test

Link Maintenance

Test Reference	Test Name
5.3.2.1	IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock
5.3.2.2	IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

Main Video Stream Reconstruction

Test Reference	Test Name
5.4.1.1	Pixel Data Reconstruction
5.4.1.2	Main Stream Data Unpacking and Unstuffing – Least Packed TU
5.4.1.3	Main Stream Data Unpacking and Unstuffing – Most Packed TU
5.4.1.4	Pixel ClockRecovery

5.4.2	Main Video Stream Format Change Handling

5.4.3.1	Entering and Exiting Power Save Mode
5.4.3.2	Resumption of Main Link Activity After Extended Idle

Main Audio Stream Reconstruction

Test Reference	Test Name
5.4.4.1	Audio Test Patterns
5.4.4.2	Audio Startup and Format Change
5.4.4.3	RS Error Correction
5.4.4.4	Audio InfoFrame Packet
5.4.4.5	Audio Clock Recovery
5.4.4.6	Audio Stream Reception

Sink FEC Protocol

Test Reference	Test Name
5.5.1.1	Sink Device FEC capability verification
5.5.1.2	Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable
5.5.1.3	Uncorrectable Block error count

5.5.1.4	Correctable Block error count
5.5.1.5	Correctable Bit error count
5.5.1.6	Correctable Parity Block error count
5.5.1.7	Correctable Parity Bit error count

DP 1.4a DSC CTS For testing Sink DUT (P/N: MT6643)

Sink Device DSC Test Procedures

Test Reference	Test Name
5.6.1.1	DSC capability verification
5.6.1.2	DSC RGB Color Depth Test
5.6.1.3	DSC RGB Block Prediction Test
5.6.1.4	DSC RGB bits-per-pixel test
5.6.1.5	DSC RGB slice test
5.6.1.6	DSC RGB lane test
5.6.1.7	DSC YcbCr 4:4:4 Color Depth Test
5.6.1.8	DSC YcbCr 4:4:4 Block Prediction Test
5.6.1.9	DSC YcbCr 4:4:4 bits-per-pixel test
5.6.1.10	DSC YcbCr 4:4:4 slice test
5.6.1.11	DSC YcbCr 4:4:4 lane test
5.6.1.12	DSC Simple 4:2:2 Color Depth Test
5.6.1.13	DSC Simple 4:2:2 Block Prediction Test
5.6.1.14	DSC Simple 4:2:2 bits-per-pixel test
5.6.1.15	DSC Simple 4:2:2 slice test
5.6.1.16	DSC Simple 4:2:2 lane test
5.6.1.17	DSC Native 4:2:2 Color Depth Test
5.6.1.18	DSC Native 4:2:2 Block Prediction Test
5.6.1.19	DSC Native 4:2:2 bits-per-pixel test
5.6.1.20	DSC Native 4:2:2 slice test
5.6.1.21	DSC Native 4:2:2 lane test
5.6.1.22	DSC Native 4:2:0 Color Depth Test
5.6.1.23	DSC Native 4:2:0 Block Prediction Test
5.6.1.24	DSC Native 4:2:0 bits-per-pixel test
5.6.1.25	DSC Native 4:2:0 slice test
5.6.1.26	DSC Native 4:2:0 lane test

Sink DSC Protocol Extension

Test Reference	Test Name
5.6.2.1	DSC Height test
5.6.2.2	DSC Padding test
5.6.2.3	DSC RGB min and max bits-per-pixel test
5.6.2.4	DSC YcbCr 4:4:4 min and max bits-per-pixel test
5.6.2.5	DSC Simple 4:2:2 min and max bits-per-pixel test
5.6.2.6	DSC Native 4:2:2 min and max bits-per-pixel test
5.6.2.7	DSC Native 4:2:0 min and max bits-per-pixel test
5.6.2.8	DSC RGB most pack test
5.6.2.9	DSC Native 4:2:2 most pack test
5.6.2.10	DSC Native 4:2:0 most pack test
5.6.2.11	DSC one corrupt slice test
5.6.2.12	DSC interrupt test for Chunk Length error
5.6.2.13	DSC interrupt test for RC buffer under-run error
5.6.2.14	DSC interrupt test for RC buffer overflow error

DP 2.1 LL CTS for testing Sink DUT (P/N MT6660)

AUX Channel Protocol

Test Reference	Test Name
5.2.1.8	Illegal AUX Request Syntax
5.2.1.9	Glitch Rejection
5.2.1.10	Interleaved EDID and DPCD Receiver Capability Read
5.2.1.11	Downstream Stop on MOT Reset
5.2.1.12	Downstream Stop on Timeout

Sink Device DPCD Field Implementation Addendum

Test Reference	Test Name
5.2.2.1	Sink Organizationally Unique Identifier (OUI)
5.2.2.2	Sink Count
5.2.2.3	Sink Status
5.2.2.5	DPCD Address Range
5.2.2.6	Number of Receiver Ports
5.2.2.7	Main Link Channel Coding
5.2.2.8	ESI Field Mapping
5.2.2.9	Sink Device Symbol Error Count
5.2.2.10	Verification of DPCD Reset Values on Upstream Device Disconnect and Power-on Reset

Link Training

Test Reference	Test Name
5.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds
5.3.1.2	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
5.3.1.3	Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure During Clock Recovery Sequence
5.3.1.4	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence
5.3.1.5	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
5.3.1.8	2-Lane Link Training CR/EQ Fallback Test
5.3.1.9	1-Lane Link Training CR/EQ Fallback Test
5.3.1.10	Successful Link Training at All Supported Lane Counts and UHBR Link Speeds
5.3.1.11	Successful Link Training to lower bandwidth, due to failure in EQ Phase of UHBR
5.3.1.12	Successful Link Training to lower bandwidth, due to failure in CDS Phase of UHBR
5.3.1.13	Successful Link Training to lower bandwidth, due to no start of CDS sequence Phase of UHBR Link Training
5.3.1.14	2-Lane UHBR Link Training EQ Fallback Test
5.3.1.15	1-Lane UHBR Link Training EQ Fallback Test

Link Maintenance

Test Reference	Test Name
5.3.2.1	IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock
5.3.2.2	IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

Main Video Stream Reconstruction

Test Reference	Test Name
5.4.1.1	8b10b Rate Pixel Data Reconstruction
5.4.1.2	8b10b Rate Main Stream Data Unpacking and Unstuffing – Least Packed TU
5.4.1.3	8b10b Rate Main Stream Data Unpacking and Unstuffing – Most Packed TU
5.4.1.4	8b10b Rate Pixel Clock Recovery
5.4.1.5	UHBR Pixel Data Reconstruction
5.4.1.6	UHBR Main Stream Data Unpacking and Unstuffing – Least Packed MTP
5.4.1.7	UHBR Main Stream Data Unpacking and Unstuffing – Most Packed MTP
5.4.1.8	UHBR Pixel Clock Recovery

Main Stream Format Change Handling

Test Reference	Test Name
5.4.2.1	8b10b Rate Main Video Stream Format Change Handling
5.4.2.2	UHBR Main Video Stream Format Change Handling

Power Management

Test Reference	Test Name
5.4.3.1	Entering and Exiting Power Save Mode
5.4.3.2	Resumption of Main Link Activity After Extended Idle
5.4.3.3	Entering and Exiting Power Save Mode at UHBR rate
5.4.3.4	Resumption of Main-Link Activity after Extended Idle at UHBR rate

Main Audio Stream Reconstruction

Test Reference	Test Name
5.4.4.1	Audio Test Patterns
5.4.4.2	Audio Startup and Format Change
5.4.4.3	RS Error Correction
5.4.4.4	Audio InfoFrame Packet
5.4.4.5	Audio Clock Recovery
5.4.4.6	Audio Stream Reception
5.4.4.7	UHBR Audio Startup and Format Change
5.4.4.8	UHBR Audio InfoFrame Packet
5.4.4.9	UHBR Audio Clock Recovery
5.4.4.10	UHBR Audio Stream Reception

Sink Handling of Split SDP testing

Test Reference	Test Name
5.4.5.1	Audio Test Patterns
5.4.5.2	Audio Startup and Format Change
5.4.5.3	RS Error Correction
5.4.5.4	Audio InfoFrame Packet
5.4.5.5	Audio Clock Recovery

Sink FEC protocol

Test Reference	Test Name
5.5.1.1	Sink Device FEC capability verification
5.5.1.2	Successful Link Training at All Supported Lane Counts and 8b10b Link Rates with FEC Enable
5.5.1.3	Uncorrectable Block error count
5.5.1.4	Correctable Block error count
5.5.1.5	Correctable Bit error count
5.5.1.6	Correctable Parity Block error count
5.5.1.7	Correctable Parity Bit error count
5.5.1.8	Aggregated Uncorrectable Block Error Count
5.5.1.9	Aggregated Correctable Block Error Count
5.5.1.10	Aggregated Correctable Bit Error Count
5.5.1.11	Aggregated Correctable Parity Block Error Count
5.5.1.2	Aggregated Correctable Parity Bit Error Count

DP 2.1 DSC CTS for Testing Sink DUT (P/N: MT6657)

Sink Device DSC Test Procedures

Test Reference	Test Name
5.6.1.1	DSC capability verification
5.6.1.2	DSC RGB Color Depth Test
5.6.1.3	DSC RGB Block Prediction Test
5.6.1.4	DSC RGB bits-per-pixel test
5.6.1.5	DSC RGB slice test
5.6.1.6	DSC RGB lane test
5.6.1.7	DSC YCbCr 4:4:4 Color Depth Test
5.6.1.8	DSC YCbCr 4:4:4 Block Prediction Test
5.6.1.9	DSC YCbCr 4:4:4 bits-per-pixel test
5.6.1.10	DSC YCbCr 4:4:4 slice test
5.6.1.11	DSC YCbCr 4:4:4 lane test
5.6.1.12	DSC Simple 4:2:2 Color Depth Test
5.6.1.13	DSC Simple 4:2:2 Block Prediction Test
5.6.1.14	DSC Simple 4:2:2 bits-per-pixel test
5.6.1.15	DSC Simple 4:2:2 slice test
5.6.1.16	DSC Simple 4:2:2 lane test

5.6.1.17	DSC Native 4:2:2 Color Depth Test
5.6.1.18	DSC Native 4:2:2 Block Prediction Test
5.6.1.19	DSC Native 4:2:2 bits-per-pixel test
5.6.1.20	DSC Native 4:2:2 slice test
5.6.1.21	DSC Native 4:2:2 lane test
5.6.1.22	DSC Native 4:2:0 Color Depth Test
5.6.1.23	DSC Native 4:2:0 Block Prediction Test
5.6.1.24	DSC Native 4:2:0 bits-per-pixel test
5.6.1.25	DSC Native 4:2:0 slice test
5.6.1.26	DSC Native 4:2:0 lane test

Sink DSC protocol extension

Test Reference	Test Name
5.6.2.1	DSC Height test
5.6.2.2	DSC Padding test
5.6.2.3	DSC RGB min and max bits-per-pixel test
5.6.2.4	DSC YCbCr 4:4:4 min and max bits-per-pixel test
5.6.2.5	DSC Simple 4:2:2 min and max bits-per-pixel test
5.6.2.6	DSC Native 4:2:2 min and max bits-per-pixel test
5.6.2.7	DSC Native 4:2:0 min and max bits-per-pixel test
5.6.2.8	DSC RGB most pack test
5.6.2.9	DSC Native 4:2:2 most pack test
5.6.2.10	DSC Native 4:2:0 most pack test
5.6.2.11	DSC one corrupt slice test
5.6.2.12	DSC interrupt test for Chunk Length error
5.6.2.13	DSC interrupt test for RC buffer under-run error
5.6.2.14	DSC interrupt test for RC buffer overflow error
5.6.2.15	Sink device handling of per slice rates and slice count capability
5.6.2.16	DSC Validation for 1/16 BPP at 8b10b Rate

Sink DSC protocol extension for UHBR Rates

Test Reference	Test Name
5.6.3.1	DSC Validation at UHBR Rates
5.6.3.2	UHBR Rate DSC RGB most pack test
5.6.3.3	UHBR Rate DSC Native 4:2:2 most pack test
5.6.3.4	UHBR Rate DSC Native 4:2:0 most pack test
5.6.3.5	Sink device handling of per slice rates and slice count capability for UHBR rate
5.6.3.6	DSC Validation for 1/16 BPP at UHBR Rate
5.6.3.7	DSC Validation for max supported pixel rate format at max UHBR Rate

DisplayID/EDID CTS for testing Sink DUT (P/N MT6647)

Note: Unigraf UCD-400 was used by VESA for TE correlation of the tests

EDID Block 0

Test Reference	Test Name
5.7.1.1	VESA E-EDID Verification Guide (Syntax Verification Only)
5.7.1.2	Physical Display Characteristics

EDID Block 0 (Basic Display Parameters and Features)

Test Reference	Test Name
5.7.1.3.1	Test for a Valid Video Input Definition
5.7.1.3.2	Test for a Valid Feature Support Byte
5.7.1.3.3	Test For Valid Established Timings I & II
5.7.1.3.4	Test For Valid Standard Timings

18-Byte Descriptor Test Cases

Test Reference	Test Name
5.7.1.4.1	Test for Detailed Timing Descriptors
5.7.1.4.2	Test for Valid Display Descriptor Structure
5.7.1.4.3	Test for Valid Display Range Limits (tag #FDh)
5.7.1.4.4	Test for Valid Standard Timing Identifier Descriptor (tag #FAh)
5.7.1.4.5	Test for Valid CVT 3 Byte Code Descriptor (tag #F8h)
5.7.1.4.6	Test for Valid Established Timings III Descriptor (tag #F7h)
5.7.1.4.7	Test for Valid String Descriptors (tags #FFh, #FEh, #FCh)
5.7.1.4.8	Unused – Reserved Data Tag Number (Tags #11h to #F6h)
5.7.1.4.9	Test for Valid Dummy Descriptors (tag #10h)

5.7.1.5	Test for Valid Extension Flag and Checksum
5.7.1.6	EDID Address A0h and A1h Handling

CTA Block Validation (CTA Extension Format)

Test Reference	Test Name
5.7.2.1	CEA Extension Version Number
5.7.2.2	Byte #2 (18-byte Descriptor Offset 'd')

Byte #3 (For CTA Extension Version 3 Only)

Test Reference	Test Name
5.7.2.3.1	Byte #3 - Underscan support
5.7.2.3.2	Byte #3 - Basic audio support
5.7.2.3.3	Byte #3 - YCbCr Support
5.7.2.3.4	Byte #3 - Native DTD Count
5.7.2.3.5	Byte #3 - Byte 3 Consistency

Data Block Collection (Type Validation)

Test Reference	Test Name
5.7.2.4.1	Duplicate Data Block Validation
5.7.2.4.2	Validity of Data Block Types

Short Video Descriptors (SVDs)

Test Reference	Test Name
5.7.2.5.1	Validity of SVDs
5.7.2.5.2	SVD/DTD Ordering

Audio Data Block

Test Reference	Test Name
5.7.2.6.1	Duplicate Audio Format Codes
5.7.2.6.2	Audio Output Validation

Speaker Allocation Data Block

Test Reference	Test Name
5.7.2.7.1	Verify Max Number of Channels

5.7.2.8	Test for Detailed Timing Descriptors

DisplayID Extension Block Framework Validation

Test Reference	Test Name
5.7.3.1	DisplayID EDID Extension Block Tag (Byte#0) and extension version (Byte#1)
5.7.3.2	DisplayID Section Size, Byte#2
5.7.3.3	DisplayID Product Identifier/ Primary Use Case, Byte#3
5.7.3.4	DisplayID Extension Count, Byte#4
5.7.3.5	DisplayID Section Checksums

DisplayID Extension Block Tiled Display Topology Block

Test Reference	Test Name
5.7.4.1	EDID – Tiled Display Block Revision (Byte#1)
5.7.4.2	EDID – Tiled Display Number of Payload Bytes in Block (Byte#2)
5.7.4.3	EDID - Tiled Display Capabilities (Byte#3, bit 6 and bit 7)
5.7.4.5	EDID - Tile Size (Byte#7 to Byte#10)

DisplayID Extension with Stereo Display Interface Data Blocks

Test Reference	Test Name
5.7.5.1	EDID – Stereo Display Interface Block Revision and Other Data (Byte #1)

DisplayID Extension with Type VII Detailed Timing Block

Test Reference	Test Name
5.7.6.1	EDID – DTD Type VII Block Revision (Byte #1)
5.7.6.2	EDID – DTD Type VII Block Number of Payload Bytes in Block (Byte #2)
5.7.6.3	EDID – DTD Type VII Block Pixel Clock (Bytes #0 through #2 of Each Descriptor)
5.7.6.4	EDID – DTD Type VII Block Descriptor Payload Verification (Bytes #3 through #19)
5.7.6.5	EDID – DTD Type VII Block Timing Support Validation

DisplayID Extension with Type VIII Detailed Timing Block

Test Reference	Test Name
5.7.7.1	EDID – DTD Type VIII Block Revision and Other Data (Byte #1)
5.7.7.2	EDID – DTD Type VIII Block Number of Payload Bytes in Block (Byte #2)
5.7.7.3	EDID – DTD Type VIII Block DMT Timing Codes
5.7.7.4	EDID – DTD Type VIII Block CTA Timing Codes
5.7.7.5	EDID – DTD Type VIII Block HDMI Timing Codes
5.7.7.6	EDID – DTD Type VIII Block Timing Support Validation

DisplayID Extension with Type IX Detailed Timing Block

Test Reference	Test Name
5.7.8.1	EDID – DTD Type IX Block Revision (Byte #1)
5.7.8.2	EDID – DTD Type IX Block Number of Payload Bytes in Block (Byte #2)
5.7.8.3	EDID – DTD Type IX Block Timing Options (Byte #0 of Each Descriptor)
5.7.8.4	EDID – DTD Type IX Block Horizontal Active Image Pixels and Vertical Active Image Lines (Bytes #1-4 of Each Descriptor)
5.7.8.5	EDID – DTD Type IX Block Refresh Rate and Pixel Clock (Byte #5 of Each Descriptor)
5.7.8.6	EDID – DTD Type IX Block Timing Support Validation

CTA Data Blocks in a DisplayID Extension

Test Reference	Test Name
5.7.9.1	Block Revision (Byte#1)
5.7.9.2	Block Number of Payload Bytes in Block (Byte#2)
5.7.9.3	Validity of Data Block Types

DisplayID Vendor-Specific Data Blocks

Test Reference	Test Name
5.7.10.1	EDID – Vendor-specific Data Block Revision (Byte #1)
5.7.10.2	EDID – Vendor-specific Data Block Number of Payload Bytes in Block (Byte #2)
5.7.10.3	EDID – Vendor-specific Data Block Manufacturer/Vendor ID Field

Dynamic Video Timing Range Limits Data Block

Test Reference	Test Name
5.7.11.1	EDID – Dynamic Video Timing Range Limits Block Revision (Byte #1)
5.7.11.2	EDID – Dynamic Video Timing Range Limits Data Block Number of Payload Bytes in Block (Byte #2)
5.7.11.3	EDID – Dynamic Video Timing Range Limits Minimum and Maximum Pixel Clocks (Bytes #3 through #8)
5.7.11.4	EDID – Dynamic Video Timing Range Limits Minimum and Maximum Vertical Refresh Rates (Bytes #9 through #11)
5.7.11.5	EDID – Dynamic Video Timing Range Limits Dynamic Video Timing Range Support Flags (Byte #11)

DisplayID Data Block Version Validation

Test Reference	Test Name
5.7.12.1	EDID - DisplayID Version 1.x Blocks
5.7.12.2	EDID - DisplayID Version 2.x Blocks
5.7.12.3	EDID - DisplayID Version 2.x Multiple Instances of Data Blocks

5.7.12.4	EDID – YCbCr 4:2:0 Consistency Validation

EDID Dynamic Refresh Rate Support with Vertical Blank Stretch with MSA_TIMING_PAR_IGNORED Option

Test Reference	Test Name
5.7.13.1	EDID – Validation
5.7.13.2	EDID – Timing Support Validation

DisplayID Extension with Type X Formula-based Timing Data Block

Test Reference	Test Name
5.7.14.1	EDID – DTD Type X Block Revision (Byte #1)
5.7.14.2	EDID – DTD Type X Block Number of Payload Bytes in Block (Byte #2)
5.7.14.3	EDID – DTD Type X Block Timing Options (Byte #0 of Each Descriptor)
5.7.14.4	EDID – DTD Type X Block Horizontal Active Image Pixels and Vertical Active Image Lines (Bytes #1-4 of Each Descriptor)
5.7.14.5	EDID – DTD Type X Block Refresh Rate and Pixel Clock (Byte #5 of Each Descriptor)
5.7.14.6	EDID – DTD Type X Block Timing Support Validation
5.7.14.7	EDID – HBlank and VBlank Validation
5.7.14.8	EDID – Alternate Minimum VBlank (Byte #7 of Each 8-byte Descriptor)

DisplayID Structure with ARVR_HMD Data Block

Test Reference	Test Name
5.7.15.1	Native DisplayID – ARVR_HMD Data Block Revision (Byte #01h)
5.7.15.2	Native DisplayID – ARVR_HMD Data Block Number of Payload Bytes in Block (Byte #02h)
5.7.15.3	Native DisplayID – ARVR_HMD Data Block Dual Layer SST Support (Byte #03h)
5.7.15.4	Native DisplayID – ARVR_HMD Data Block Number of Displays and Streams (Byte #04h)
5.7.15.5	Native DisplayID – ARVR_HMD Data Block Layers (Byte #05h)
5.7.15.6	Native DisplayID – ARVR_HMD Data Block Area of Low Distortion (Bytes #06h through #12h)
5.7.15.7	Native DisplayID – ARVR_HMD Data Block Lenses (Byte #19h)
5.7.15.8	Native DisplayID – ARVR_HMD Data Block Lens Adjustments Available in HMD and Foveated Rendering Support (Bytes #24h and #25h)
5.7.15.9	Native DisplayID – ARVR_HMD Data Block Center of Projection (Bytes #40h through #4Fh)
5.7.15.10	Native DisplayID – ARVR_HMD Data Block Streams_per_Layer (Bytes #50h and #51h)
5.7.15.11	Native DisplayID – HMD Mandate for ARVR_HMD Data Block

DisplayID Structure with ARVR_Layer Data Block

Test Reference	Test Name
5.7.16.1	Native DisplayID – ARVR_Layer Data Block Revision (Byte #01h)
5.7.16.2	Native DisplayID – ARVR_Layer Data Block Number of Payload Bytes in Block (Byte #02h)
5.7.16.3	Native DisplayID – ARVR_Layer Data Block Consistency
5.7.16.4	Native DisplayID – ARVR_Layer Data Block Layers (Byte #0Ch)
5.7.16.5	Native DisplayID – ARVR_Layer Data Block RESERVED (For Tile Location) (Byte #0Dh)
5.7.16.6	Native DisplayID – ARVR_Layer Data Block Lens Distortion (Byte #0Eh)
5.7.16.7	Native DisplayID – ARVR_Layer Data Block Asynchronous Reprojection (Byte #10h)

5.7.16.9	Native DisplayID – ARVR_Layer Data Block Multiple Stream Stereo Modes (Byte #16h)
5.7.16.10	Native DisplayID – HMD Mandate for ARVR_Layer Data Block

DisplayID Extension with Adaptive-Sync Data Block

Test Reference	Test Name
5.7.17.1	EDID – Adaptive-Sync Data Block Revision and Descriptor Size (Byte #1)
5.7.17.2	EDID – Adaptive-Sync Data Block Number of Payload Bytes in Block (Byte #2)
5.7.17.3	EDID – Adaptive-Sync Data Block Adaptive-Sync Operation Mode and Range Descriptor RESERVED Values (Bytes #0 and #4 of Each Descriptor)
5.7.17.4	EDID – Adaptive-Sync Data Block Minimum and Maximum Refresh Rates (Bytes #2 through #4 of Each Descriptor)
5.7.17.5	EDID – Adaptive-Sync/CVT Timing Match Validation

Sink Device Native DisplayID Test Procedures

Test Reference	Test Name
5.7.18.1	Block Revision and Descriptor Size (Byte #1)

Native DisplayID Framework Validation

Test Reference	Test Name
5.7.19.1	Native DisplayID – Structure Version/Revision (Byte 00h)
5.7.19.2	Native DisplayID – Bytes in Section (Byte 01h)
5.7.19.3	Native DisplayID – Product Identifier / Display Product Primary Use Case (Byte 02h)
5.7.19.4	Native DisplayID – Extension Count (Byte 03h)
5.7.19.5	Native DisplayID – Section Checksums
5.7.19.6	Native DisplayID – Mandatory Blocks

Product Identification Data Block

Test Reference	Test Name
5.7.20.1	Native DisplayID – Product Identification Data Block Revision (Byte 1)
5.7.20.2	Native DisplayID – Product Identification Data Block Number of Payload Bytes in Block (Byte 2)
5.7.20.3	Native DisplayID – Product Identification Data Block Week of Manufacture/Model Tag and Year of Manufacture/Model Year (Bytes 12 and 13)

Display Parameters Data Block

Test Reference	Test Name
5.7.21.1	Native DisplayID – Display Parameters Data Block Revision (Byte 1)
5.7.21.2	Native DisplayID – Display Parameters Data Block Number of Payload Bytes in Block (Byte 2)
5.7.21.3	Native DisplayID – Display Parameters Data Block Feature Support Flags Field (Byte 0Bh)
5.7.21.4	Native DisplayID – Display Parameters Data Block Native Luminance-related Fields (Bytes 18h to 1Dh)
5.7.21.5	Native DisplayID – Display Parameters Data Block Native Color Depth and Display Device Technology Fields (Byte 1Eh)

Display Interface Data Block

Test Reference	Test Name
5.7.22.1	Native DisplayID – Display Interface Features Data Block Revision (Byte 1)
5.7.22.2	Native DisplayID – Display Interface Features Data Block Number of Payload Bytes in Block (Byte 2)

5.7.22.3	Native DisplayID – Display Interface Features Data Block Supported Interface Color Depth-related Fields
5.7.22.4	Native DisplayID – Display Interface Features Data Block Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported (Byte 7)
5.7.22.5	Native DisplayID – Display Interface Features Data Block Supported Interface Audio Capability and Feature Flags (Byte 8)
5.7.22.6	Native DisplayID – Display Interface Features Data Block Supported Interface Color Space and EOTF-related Fields
5.7.22.7	Native DisplayID – Display Interface Features Data Block Additional Supported Interface Color Space and EOTF-related Fields (Bytes 0Bh to 12h)

Adaptive-Sync CTS for testing Sink DUT (P/N: MT6649)

Note: Unigraf UCD-400 was used by VESA for TE correlation of the tests

Adaptive-Sync Operation Validation

Test Reference	Test Name
5.8.1.1	Fixed-Average VTotal Mode Support over the Declared Frame Rate Range
5.8.1.2	Duration Increase and Decrease Constraint Value Support in Adaptive VTotal Mode
5.8.1.3	Adaptive VTotal Mode Support

LTTPR CTS for Testing Sink DUT (P/N: MT6679)

Sink Embedded LTTPR protocol

Test Reference	Test Name
5.9.1.1	LTTPR global configuration verification
5.9.1.2	LTTPR configuration and status field verification
5.9.1.3	LTTPR AUX read/write reply time budget verification
5.9.1.4	LTTPR 8b10b transparent link training for lane count and link rate
5.9.1.5	LTTPR 8b10b non-transparent link training for lane count and link rate
5.9.1.6	LTTPR 128b132b non-transparent link training for lane count and link rate
5.9.1.7	LTTPR 8b10b transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)
5.9.1.8	LTTPR 8b10b non-transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)
5.9.1.9	LTTPR 8b10b transparent successful Link Training (Lower Link bandwidth During Clock Recovery)
5.9.1.10	LTTPR 8b10b non-transparent successful Link Training (Lower Link bandwidth During Clock Recovery)
5.9.1.11	LTTPR 8b10b transparent successful Link Training (Lower Link Bandwidth Channel Equalization)
5.9.1.12	LTTPR 8b10b non-transparent successful Link Training (Lower Link Bandwidth Channel Equalization)
5.9.1.13	LTTPR 128b132b non-transparent successful Link Training to Lower Link Rate due to failure in EQ Phase of UHBR
5.9.1.14	LTTPR 128b132b non-transparent successful Link Training to Lower Link Rate due to failure in CDS Phase of UHBR
5.9.1.15	LTTPR 128b132b non-transparent successful Link Training to lower bandwidth due to no start of CDS sequence Phase of UHBR Link Training

4. DP 2.1 LTTPR DUT TESTS

DP 2.1 LTTPR CTS for testing LTTPR Device (P/N MT6681)

LTTPR and DP Tunnel Device Test Procedures

LTTPR Device Capabilities validation tests

Test Reference	Test Name
7.1.1.1	Data structure revision validation
7.1.1.2	Phy repeater count validation
7.1.1.3	Phy repeater lane count validation
7.1.1.4	Phy repeater link rate validation
7.1.1.5	Phy repeaters DPCD register validation at various LTTPR position
7.1.1.6	Phy repeater AUX read/write time budget validation
7.1.1.7	OUI and Device Identification string validation at various LTTPR position
7.1.1.8	Phy repeater Downspread (DPCD 00107h) write validation
7.1.1.9	Phy repeater retry on No-Reply during AUX Read in LTTPR mode

LTTPR 8b10b Transparent Link Training validation tests

Test Reference	Test Name
7.1.2.1	With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.2	With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.3	With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.4	With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.5	With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.6	With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.7	With 0 emulated LTTPR, With SSC enable Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Transparent mode
7.1.2.8	With 0 emulated LTTPR, Link Training with UFP fails when DFP not able to do clock lock at max supported Lane Count and 8b10b Link Speed in Transparent mode
7.1.2.9	With 0 emulated LTTPR, Link Training with UFP fails when DFP not able to do symbol lock at max supported Lane Count and 8b10b Link Speed in Transparent mode

LTTPR 8b10b Non-Transparent Link Training validation tests

Test Reference	Test Name
7.1.3.1	With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.2	With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.3	With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode

7.1.3.4	With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.5	With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.6	With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.7	With 0 emulated LTTPR, With SSC enable Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-Transparent mode
7.1.3.8	With 0 emulated LTTPR, Successful transition between Transparent and Non-Transparent Link Training at max Supported Lane Counts and 8b10b Link Speeds

LTTPR 128b132b Non-Transparent Link Training validation tests

Test Reference	Test Name
7.1.4.1	With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.2	With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.3	With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.4	With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.5	With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.6	With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.7	With 0 emulated LTTPR, With SSC enable Successful Link Training at all Supported Lane Counts and UHBR Link Speeds in Non-Transparent mode
7.1.4.8	With 0 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b132b Link Speeds in Non- Transparent mode
7.1.4.9	With 5 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode
7.1.4.10	With 5 emulated LTTPR, Link Training with successful link training at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode

LTTPR 8b10b Symbol error validation tests

Test Reference	Test Name
7.1.5.1	With 0 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate
7.1.5.2	With 1 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate
7.1.5.3	With 2 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate
7.1.5.4	With 3 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate
7.1.5.5	With 4 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate
7.1.5.6	With 5 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate

LTTPR 8b10b FEC status and error validation tests

Test Reference	Test Name
7.1.6.1	With 0 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.2	With 1 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.3	With 2 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.4	With 3 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.5	With 4 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.6	With 5 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate
7.1.6.7	With 0 emulated LTTPR, Reference Sink FEC status and error counter validation at max supported lane count and 8b10b link rate, when LTTPR DUT is FEC unaware

LTTPR 128b132b FEC status and error validation tests

Test Reference	Test Name
7.1.7.1	With 0 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.2	With 1 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.3	With 2 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.4	With 3 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.5	With 4 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.6	With 5 emulated LTTPR, FEC status and error counter validation at max supported lane count and 128b132b link rate
7.1.7.7	With 0 emulated LTTPR, Reference Sink FEC status and error counter validation at max supported lane count and 8b10b link rate, when LTTPR DUT is FEC unaware

LTTPR 8b10b Non-LTTPR Link Training validation tests

Test Reference	Test Name
7.1.8.1	With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link Speeds in Non-LTTPR mode

LTTPR DSC validation tests for SST and MST

Test Reference	Test Name
7.1.9.1	With 0 emulated LTTPR, Successful Link Training after IRQ HPD

LTTPR DSC validation tests for SST and MST

Test Reference	Test Name
7.1.10.1	LTTPR DSC validation test over SST
7.1.10.2	LTTPR DSC validation test over MST with 4 VCs

LTTPR HDCP validation tests for SST and MST

Test Reference	Test Name
7.1.11.1	LTTPR DSC validation test over SST
7.1.11.2	LTTPR DSC validation test over MST with 4 VCs

LTTPR Split SDP validation tests

Test Reference	Test Name
7.1.12.1	LTTPR Capability to handle split VSC SDP over MSA
7.1.12.2	LTTPR Capability to handle split VSC SDP over first vertical blanking
7.1.12.3	LTTPR Capability to handle split VSC SDP over last vertical blanking
7.1.12.4	LTTPR Capability to handle split PPS SDP over vertical blanking
7.1.12.5	LTTPR Capability to handle split PPS SDP over last vertical blanking
7.1.12.6	LTTPR Capability to handle split Custom SDP over multiple vertical blanking
7.1.12.7	LTTPR Capability to handle split Custom SDP over last vertical blanking and multiple horizontal blanking
7.1.12.8	LTTPR Capability to handle split Custom SDP over last horizontal blanking rest on next frame vertical blank

DP Tunnel Device Test Procedures

DP Tunnel error counter validation tests

Test Reference	Test Name
7.2.1.1	With 0 emulated LTTPR, Symbol error counter validation at max supported lane count and 8b10b link rate in Non-Transparent mode
7.2.1.2	With 0 emulated LTTPR, FEC status and error counter validation at max supported lane count and 8b10b link rate in Non-Transparent mode

5. HDCP CTS FOR DISPLAYPORT

DP HDCP 2.3 CTS Capable Hardware Products

Product	P/N	Description
UCD-500 Gen2 DP 2.1 Test Device	066710	DisplayPort™ 2.1 Video Generator and Analyzer unit for testing DisplayPort Sinks and Sources up to 8K@60Hz and 16K@60 Hz (with DSC) video modes with UHBR 20 Max Bit Rate Capability.

DP HDCP 2.3 CTS Test Software Product Options

Product	P/N	Description
HDCP 2.3 CTS for testing Source DUT on DP	MT6634	HDCP 2.3 on DisplayPort compliance tests for testing Source DUT. (Sets 1A + 1B)
HDCP 2.3 CTS for testing Sink DUT on DP	MT6636	HDCP 2.3 on DisplayPort compliance tests for testing Sink DUT. (Set 2C)
HDCP 2.3 CTS for Repeater DUT on DP	MT6638	HDCP 2.3 on DisplayPort CTS for testing Sink, Source and Repeater DUT. (Sets 1A + 1B + 2C + 3A + 3B + 3C)

Description of HDCP 2.3 CTS Tests

Note:	With SW version 2.3 HDCP is supported only when 8b/10b link coding is enabled

DP HDCP 2.3 CTS for testing Source DUT (P/N MT6634)

1A. Downstream procedure with Receiver

Test Reference	Test Name
HDCP2.3 CTS 1A-01	Regular Procedure – With previously connected Receiver (With stored km)
HDCP2.3 CTS 1A-02	Regular Procedure – With newly connected Receiver (Without stored km)
HDCP2.3 CTS 1A-03	Regular Procedure – Receiver disconnect after AKE_Init
HDCP2.3 CTS 1A-04	Regular Procedure – Receiver disconnect after km
HDCP2.3 CTS 1A-05	Regular Procedure – Receiver disconnect after locality check
HDCP2.3 CTS 1A-06	Regular Procedure – Receiver disconnect after ks
HDCP2.3 CTS 1A-07	Regular Procedure – Receiver sends REAUTH_REQ after ks
HDCP2.3 CTS 1A-08	Irregular Procedure – Verify Receiver Certificate
HDCP2.3 CTS 1A-09	Irregular Procedure – SRM
HDCP2.3 CTS 1A-10	Irregular Procedure – Invalid H'
HDCP2.3 CTS 1A-11	Irregular Procedure – Pairing Failure
HDCP2.3 CTS 1A-12	Irregular Procedure – Locality Failure

1B. Downstream procedure with Repeater

HDCP2.3 CTS 1B-01	Regular Procedure – With Repeater
HDCP2.3 CTS 1B-02	Irregular Procedure – Timeout of Receiver ID list
HDCP2.3 CTS 1B-03	Irregular Procedure – Verify V'
HDCP2.3 CTS 1B-04	Irregular Procedure – MAX_DEVS_EXCEEDED
HDCP2.3 CTS 1B-05	Irregular Procedure – MAX CASCADE_EXCEEDED
HDCP2.3 CTS 1B-06	Irregular Procedure – Incorrect *seq_num_V*
HDCP2.3 CTS 1B-07	Regular Procedure – Re-authentication on HPD
HDCP2.3 CTS 1B-08	Regular Procedure – Re-authentication on REAUTH_REQ
HDCP2.3 CTS 1B-09	Irregular Procedure – Rollover of *seq_num_V*
HDCP2.3 CTS 1B-10	Irregular Procedure – Failure of Content Stream Management

DP HDCP 2.3 CTS for testing Sink DUT (P/N MT6636)

Note: With SW version 2.3 HDCP is supported only when 8b/10b link coding is enabled

2C. Upstream procedure with Transmitter

Test Reference	Test Name
HDCP2.3 CTS 2C-01	Regular Procedure – With transmitter
HDCP2.3 CTS 2C-02	Irregular Procedure – New Authentication after AKE_Init
HDCP2.3 CTS 2C-03	Irregular Procedure – New Authentication during Locality Check
HDCP2.3 CTS 2C-04	Irregular Procedure – New Authentication after SKE_Send_Eks
HDCP2.3 CTS 2C-05	Irregular Procedure – New Authentication during Link Synchronization

DP HDCP 2.3 CTS for testing Sink, Source and Repeater DUT (P/N MT6638)

Note: With SW version 2.3 HDCP is supported only when 8b/10b link coding is enabled

1A. Downstream procedure with Receiver

Please see above

1B. Downstream procedure with Repeater

Please see above

2C. Upstream procedure with Transmitter

Please see above

3A. Downstream procedure with Receiver

Test Reference	Test Name
HDCP2.3 CTS 3A-01	Regular Procedure – With previously connected Receiver (With stored k_m)
HDCP2.3 CTS 3A -02	Regular Procedure – With newly connected Receiver (Without stored k_m)
HDCP2.3 CTS 3A -03	Irregular Procedure – Verify Receiver Certificate
HDCP2.3 CTS 3A -04	Irregular Procedure – invalid H'
HDCP2.3 CTS 3A -05	Irregular Procedure – Pairing Failure
HDCP2.3 CTS 3A -06	Irregular Procedure – Locality Failure

3B. Downstream Procedure with Repeater

HDCP2.3 CTS 3B-01	Regular Procedure – With Repeater
HDCP2.3 CTS 3B -02	Irregular Procedure – Timeout of Receiver ID list
HDCP2.3 CTS 3B -03	Irregular Procedure – Verify V'
HDCP2.3 CTS 3B -04	Irregular Procedure – MAX_DEVS_EXCEEDED
HDCP2.3 CTS 3B -05	Irregular Procedure – MAX_CASCADE_EXCEEDED
HDCP2.3 CTS 3B -06	Irregular Procedure – Rollover of *seq_num_V*
HDCP2.3 CTS 3B -07	Irregular Procedure – Failure of Content Stream Management

3C. Downstream Procedure with Transmitter

Test Reference	Test Name
HDCP2.3 CTS 3C-01	Regular Procedure – Transmitter – DUT – Receiver
HDCP2.3 CTS 3C -02	Regular Procedure – Receiver Disconnect Propagation when an Active Receiver is Disconnected Downstream
HDCP2.3 CTS 3C -03	Regular Procedure – Receiver Connected when an Active Receiver is Connected Downstream
HDCP2.3 CTS 3C -04	Irregular Procedure – New Authentication after AKE_init
HDCP2.3 CTS 3C -05	Irregular Procedure – New Authentication during Locality Check
HDCP2.3 CTS 3C -06	Irregular Procedure – New Authentication after SKE_Send_Eks
HDCP2.3 CTS 3C -07	Irregular Procedure – New Authentication during Link Synchronization
HDCP2.3 CTS 3C -08	Irregular Procedure – Rx Certificate invalid
HDCP2.3 CTS 3C -09	Irregular Procedure – invalid H'
HDCP2.3 CTS 3C -10	Irregular Procedure – Locality Failure
HDCP2.3 CTS 3C-11	Regular Procedure – Transmitter – DUT – Repeater (With stored km)
HDCP2.3 CTS 3C-12	Regular Procedure – Receiver disconnect after AKE_Init
HDCP2.3 CTS 3C-13	Regular Procedure – Receiver disconnect after km
HDCP2.3 CTS 3C-14	Regular Procedure – Receiver disconnect after locality check
HDCP2.3 CTS 3C-15	Regular Procedure – Receiver disconnect after Ks
HDCP2.3 CTS 3C-16	Irregular Procedure – Timeout of Receiver ID list
HDCP2.3 CTS 3C-17	Irregular Procedure – Verify V'
HDCP2.3 CTS 3C-18	Irregular Procedure – DEVICE_COUNT
HDCP2.3 CTS 3C-19	Irregular Procedure – DEPTH
HDCP2.3 CTS 3C-20	Irregular Procedure – MAX_DEVS_EXCEEDED
HDCP2.3 CTS 3C-21	Irregular Procedure – MAX_CASCADE_EXCEEDED
HDCP2.3 CTS 3C-22	Regular Procedure – Repeater with zero downstream device
HDCP2.3 CTS 3C-23	Regular Procedure – Propagation of HDCP2_0_REPEATER_DOWNSTREAM flag
HDCP2.3 CTS 3C-24	Regular Procedure – Propagation of HDCP1_DEVICE_DOWNSTREAM flag
HDCP2.3 CTS 3C-25	Regular Procedure – Content Stream Management