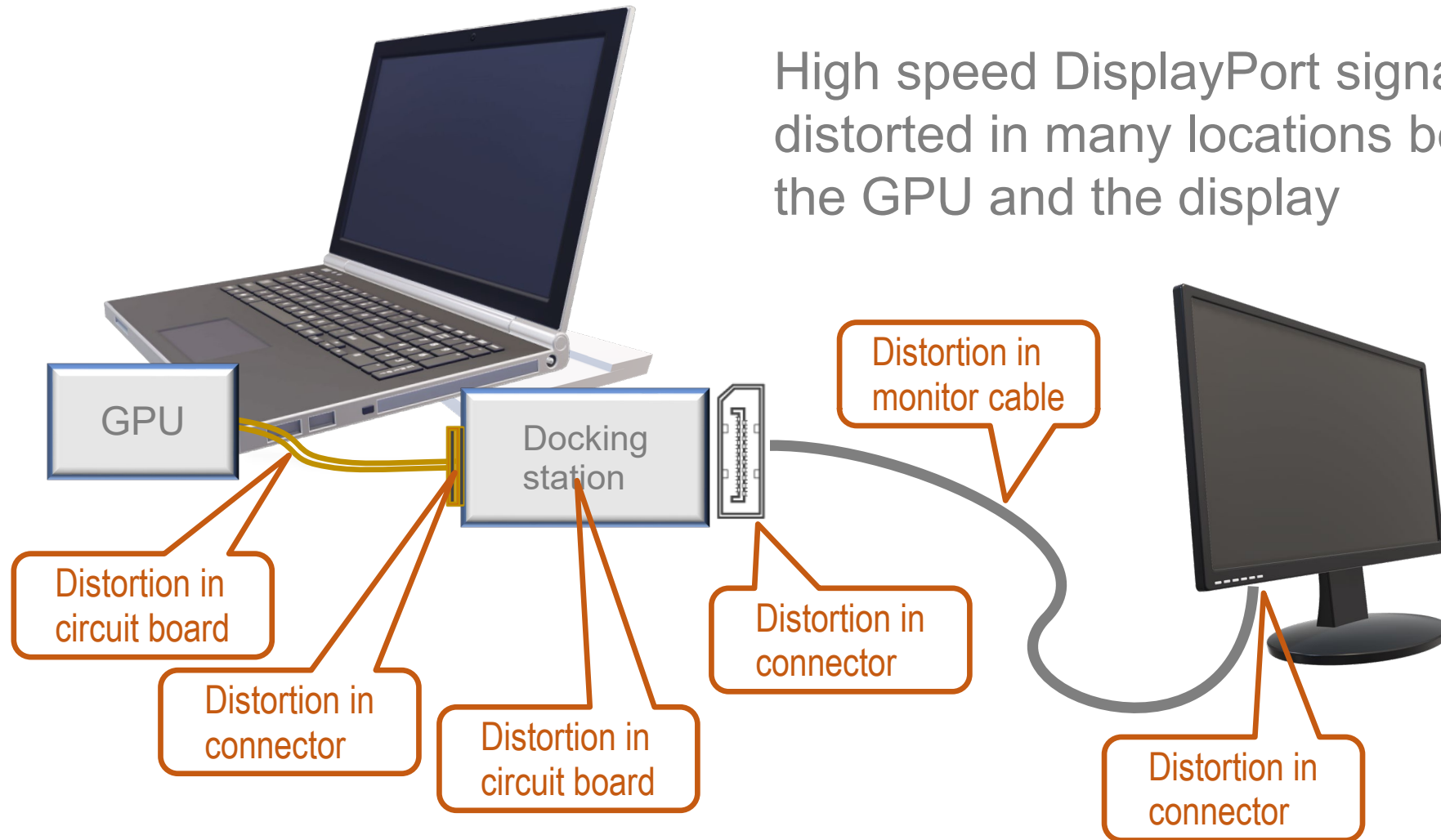# Introduction to LTTPR in DP 1.4a applications

Link-Training Tunable PHY Repeaters

- This presentation describes LTTPR in **DP 1.4a applications**
- For details about LTTPR in DP 2.1 applications, please [contact Unigraf](#).

- What is a Link-Training Tunable PHY Repeater (LTTPR)?
- Why would you need a repeater?
- LTTPR features

- Example:
  - ✓ Recognizing LTTPRs
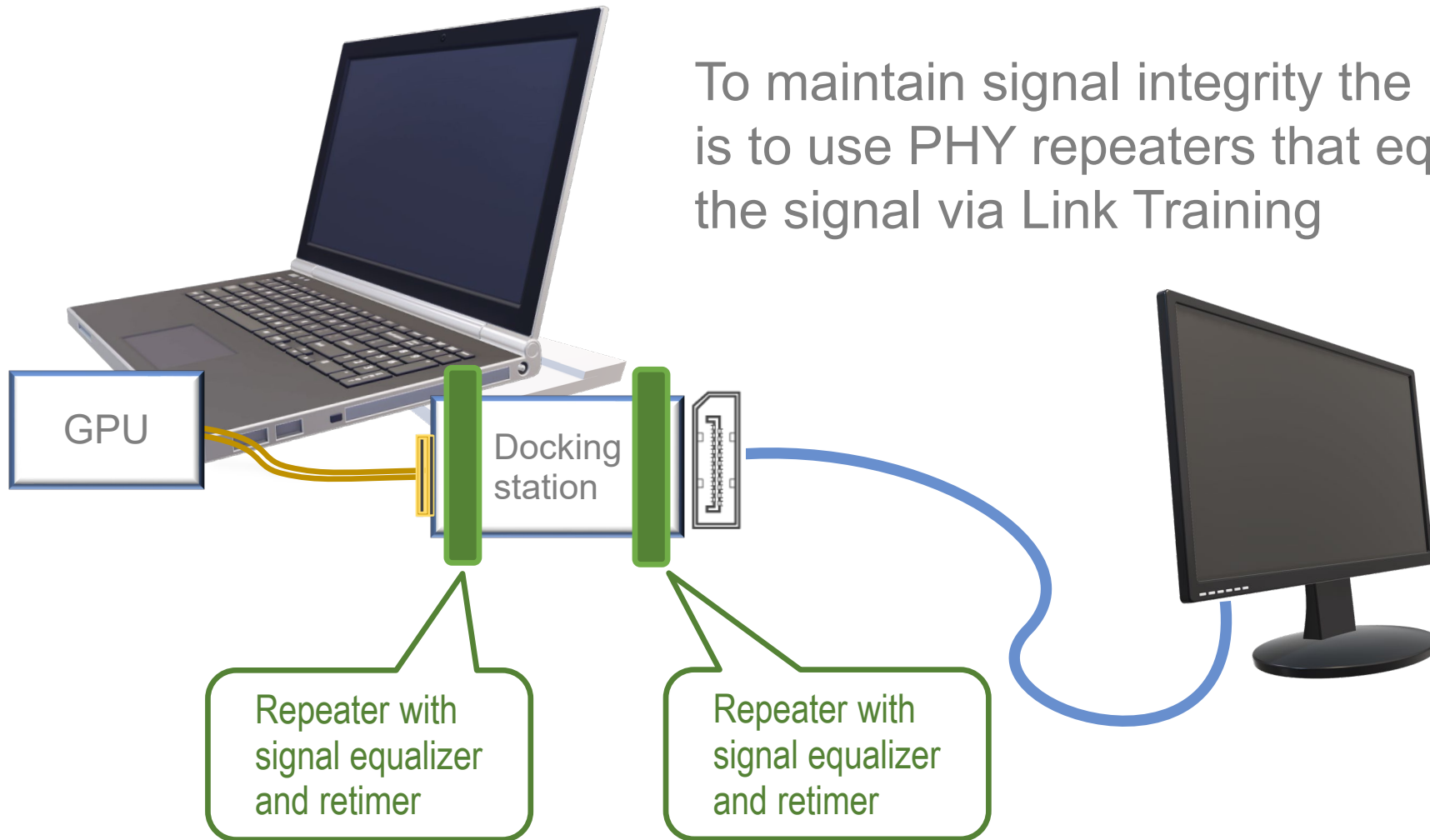 - ✓ Link training with LTTPRs

PHY Repeaters

- A **PHY repeater** is a device containing only the PHY layer of data receiver and data transmitter for cleaning up signal waveform distortion caused by transmission across a cable, connector, or circuit board traces
- A PHY repeater does not contain encryption layer

- A PHY repeater that is capable of adjusting its output for Link Training is called Link-Training Tunable PHY Repeater

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Why LTTPR?

UNIGRAF

High speed DisplayPort signal is distorted in many locations between the GPU and the display

GPU

Docking station

Distortion in circuit board

Distortion in connector

Distortion in circuit board

Distortion in connector

Distortion in monitor cable

Distortion in connector

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Why LTTPR?

To maintain signal integrity the best option is to use PHY repeaters that equalize the signal via Link Training

GPU

Docking station

Repeater with signal equalizer and retimer

Repeater with signal equalizer and retimer

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PHY Repeater Ensures Signal Integrity

- DisplayPort's high 8.1 Gbps/lane bit rate requires an active cable with PHY repeaters for cable lenghts exceeding 2 m .
- A USB Type-C cable longer than 1 m must have PHY repeaters to provide full performance.
  - ✓ Desktop computer connections typically require 2 m cables.
- Docking stations or "mini-docks" of laptop computers and USB Type-C connected equipment also need PHY repeaters

LTTPR Features

- LTTPR contains DP RX and DP TX PHY and a signal retimer
- LTTPR contains means for tuning the PHY parameters during LT
- LTTPR has up to four main Link Lanes and full Voltage Swing and Pre-emphasis combinations
- Specific DPCD register range (F0000h – F028Fh) for LTTPR use
- Up to 8 LTTPRs can be placed in the data path between DP Source, DP Sink or DP Repeater devices
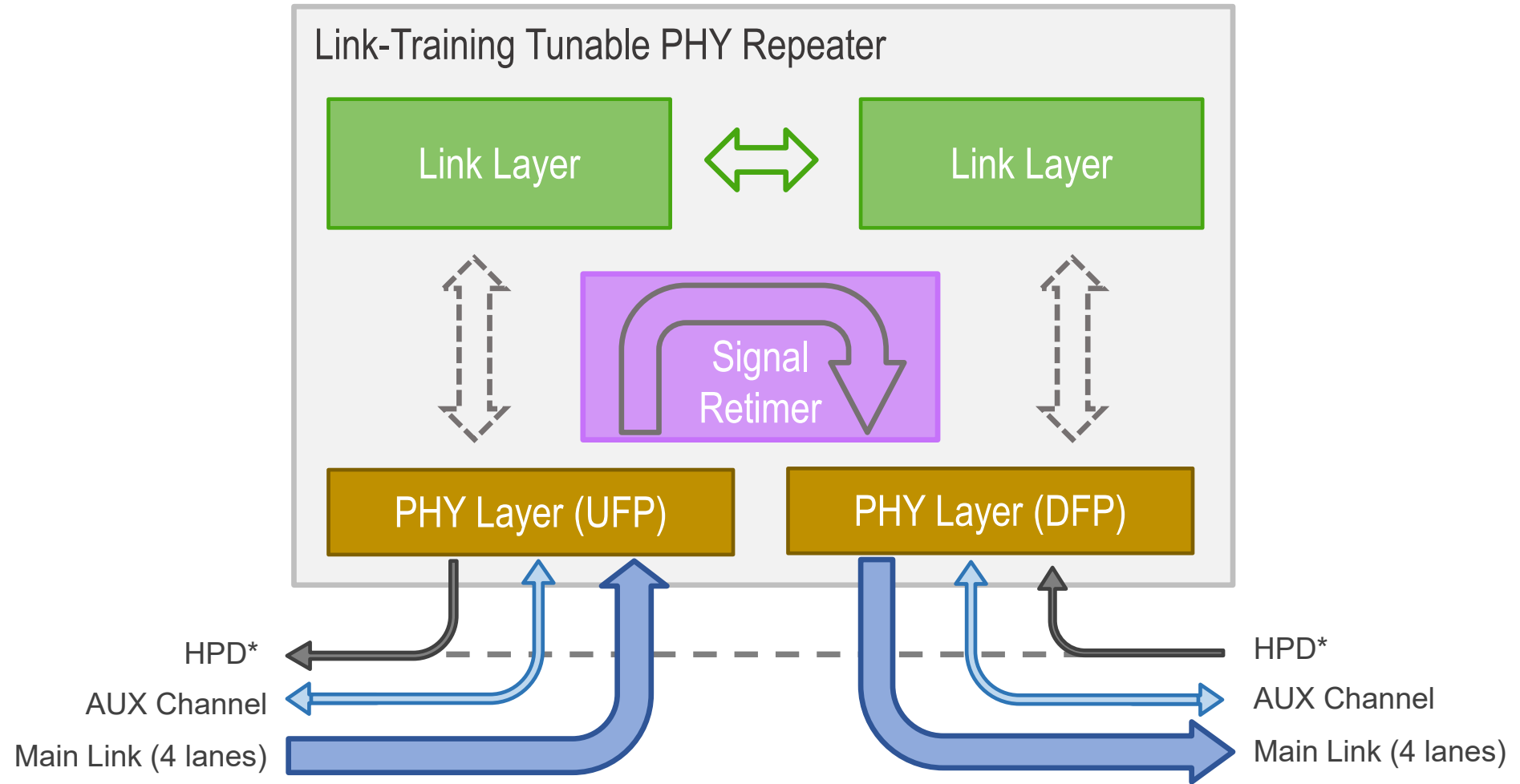
Two Operating Modes

Transparent Mode:
- Passes through all AUX transactions
- Snoops transactions to DPCD 00100h – 002FFh and updates output as needed

Non-transparent Mode:
- Replies to AUX transactions to LTTPR specific DPCD fields
- Passes through all other transactions
- Snoops transactions to DPCD 00100h – 002FFh and updates output as needed

DP Source controls LTTPR operating modes

LTTPR DPCD Registers

00000h – 000FFh
00100h – 002FFh
…
F0000h – F000Fh
F0010h – F005Fh
F0060h – F00AFh
…
F0240h – F028Fh
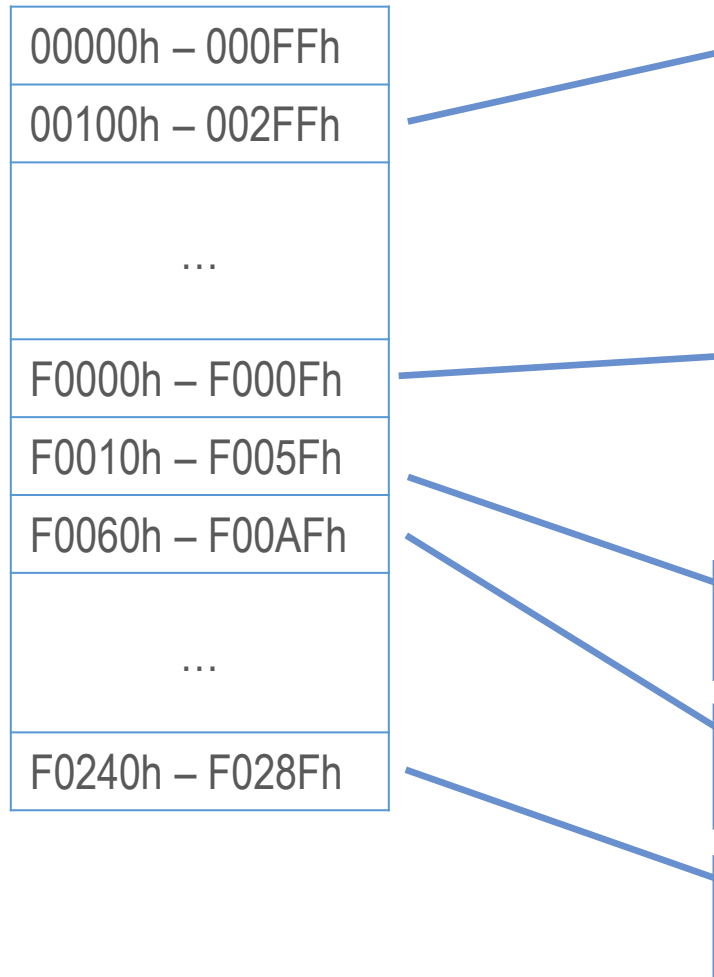
Link Configuration and Link/Sink Device Status

- *All LTTPRs shall snoop AUX transactions to these registers*
- *LTTPRs in Transparent Mode shall update output as needed*
- *LTTPR1 in Non-Transparent Mode shall update output as needed*

LT-tunable PHY Repeater DPCD Capability and ID Field

- *Shared by all LTTPRs between a DPTX and DPRX*
- *All LTTPRs shall replay to AUX transactions to these registers*

PHY_Repeater1 Configuration and Status
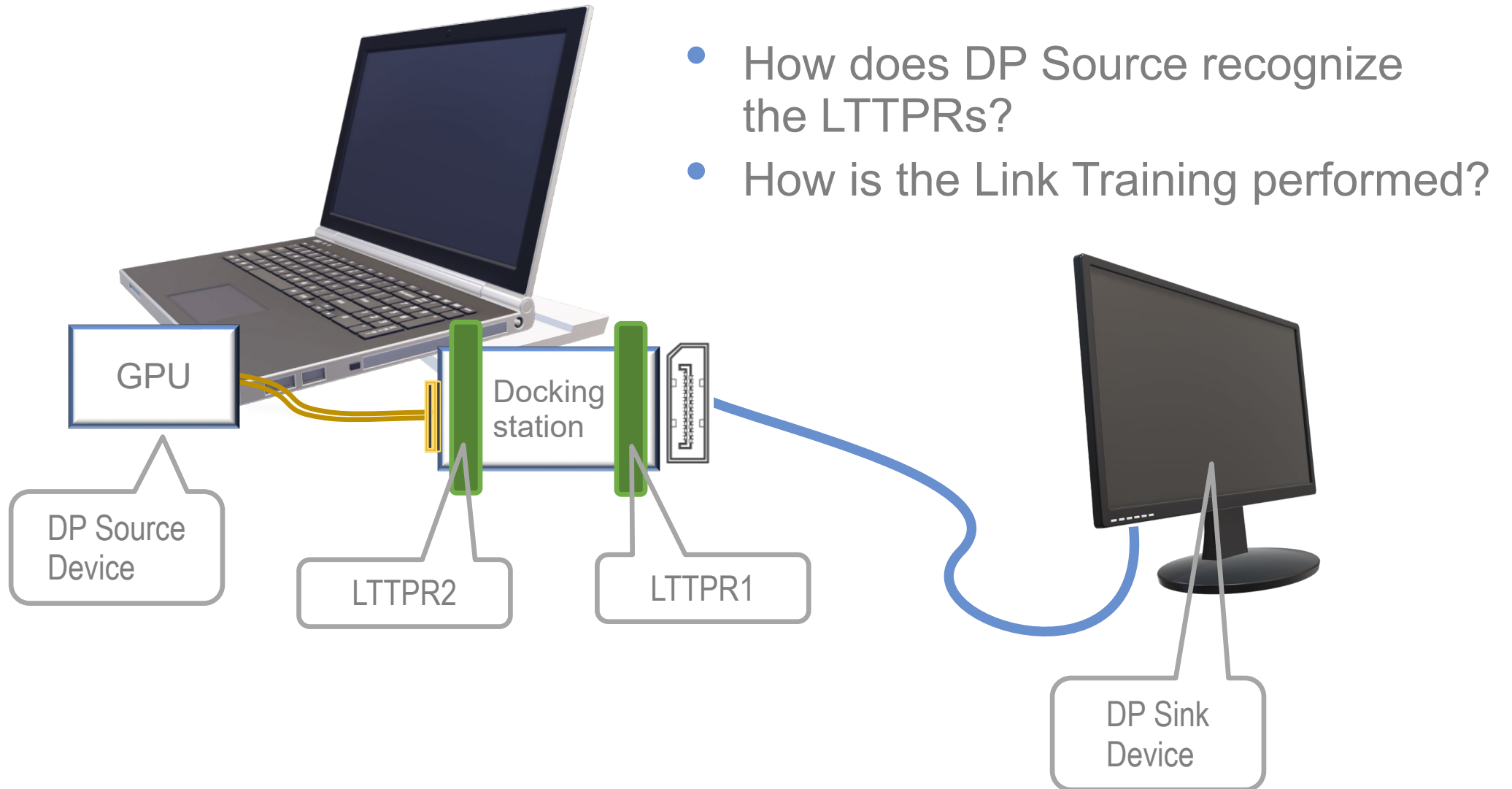
- *Only LTTPR1 replies AUX transactions to these registers*

PHY_Repeater2 Configuration and Status

- *Only LTTPR2 replies AUX transactions to these registers*

PHY_Repeater8 Configuration and Status

- *Only LTTPR8 replies AUX transactions to these registers*

Example Configuration

- How does DP Source recognize the LTTPRs?
- How is the Link Training performed?

GPU

Docking station

DP Source Device

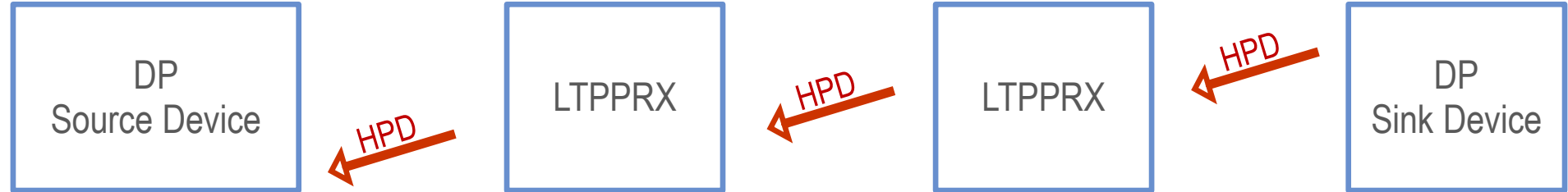LTTPR2

LTTPR1

DP Sink Device

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LTTPR Recognition

- Phase 1 (HPD is propagated):
  - ✓ HPD is asserted by DP Sink. All LTTPRs pass the signal.
- Phase 2 (Repeater count and capabilities):
  - ✓ DP Source reads DPCD F0000h to F0004h
  - ✓ DP Sink replies with zero data
  - ✓ LTTPR that receives zero count (LTTPR1) replaces it with its own data
  - ✓ Each LTTPR update the data with their capabilities and increment the count
- Phase 3 (DP Sink capabilities)
  - ✓ DP Source reads DPCD 00000h to 00002h
  - ✓ DP Sink replies with its capability data
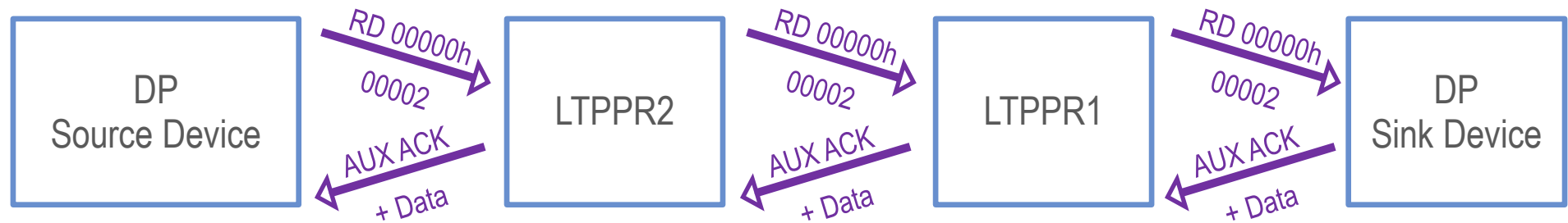 - ✓ Each LTTPR pass the information
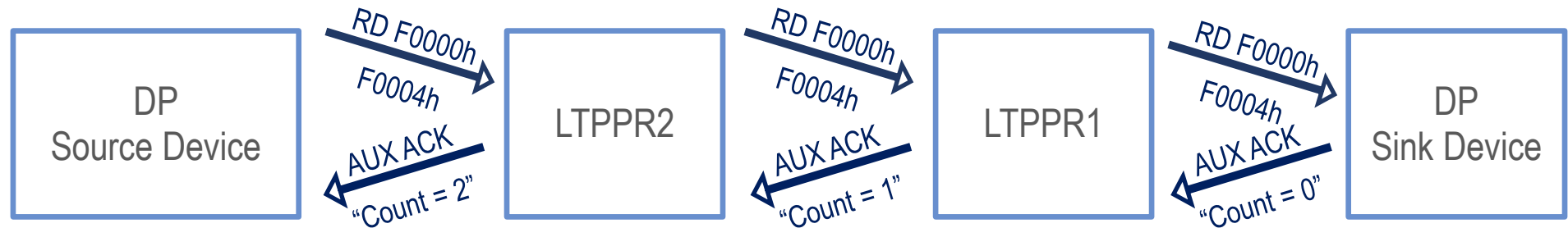
Link Training with LTTPRs

- DP Source performs full LT with each of the LTTPRs
  - ✓ LT starts with repeater closest to DP Source and ends with repeater closest to DP Sink
- DP Source writes to LTTPR specific LT registers
  - ✓ DP Sink and non-adressed LTTPRs reply AUX_NACK with M = 0
- DP Source reads LTTPR specific LT registers
  - ✓ DP Sink and non-adressed LTTPRs reply AUX_ACK with zero or copy data
- The LTTPR closest upstream snoops the data and sets its output accordingly
- When all LTTPRs have been trained, DP Source LT with DP Sink
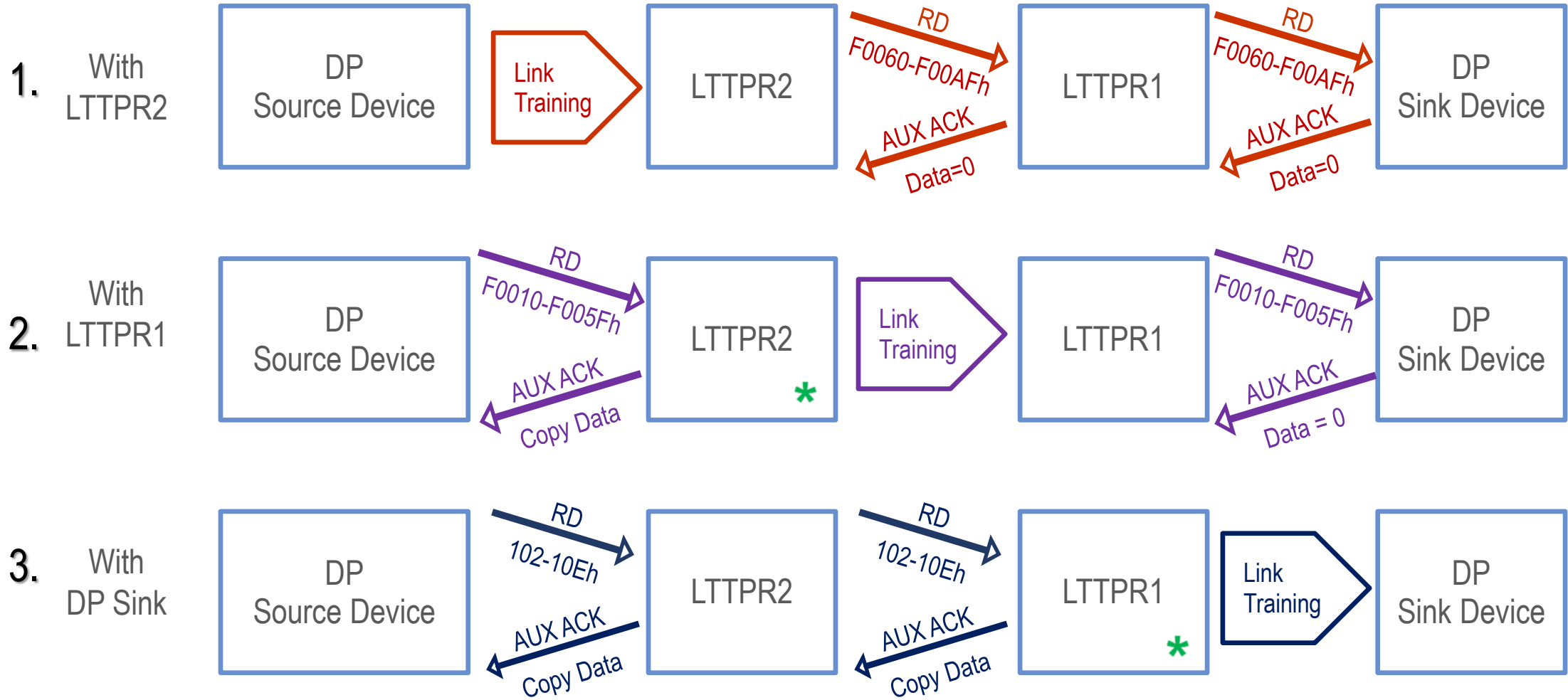
# Unigraf UCD-400 Tester Supports LTTPR

- UCD-400 Features
  - ✓ Test DisplayPort 1.4a / HBR3 Sinks, Sources and Repeaters
  - ✓ Capture and Source up to 8K@30 & 4K@120 video and audio
  - ✓ Verify HDCP 1.3 and HDCP 2.3 operation; Run HDCP 2.3 Compliance Test
  - ✓ Monitor link status, set configuration parameters
  - ✓ USB 3.0 connected
- *UCD Console* GUI for debugging
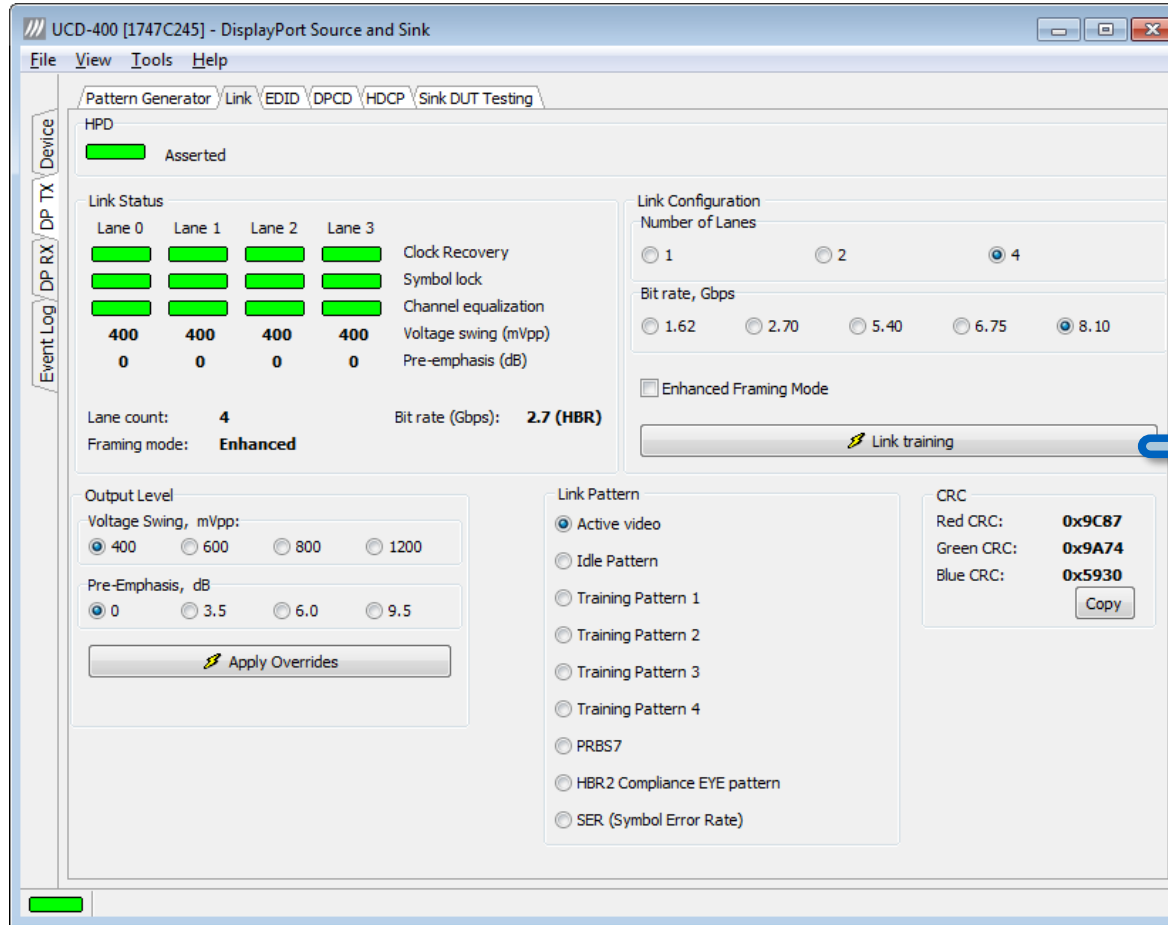- High level *TSI API* for easy integration

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UCD Console GUI

Reference Sink
(Test Source DUT)

Reference Source
(Test Sink DUT)

CAPTURING THE WORLD
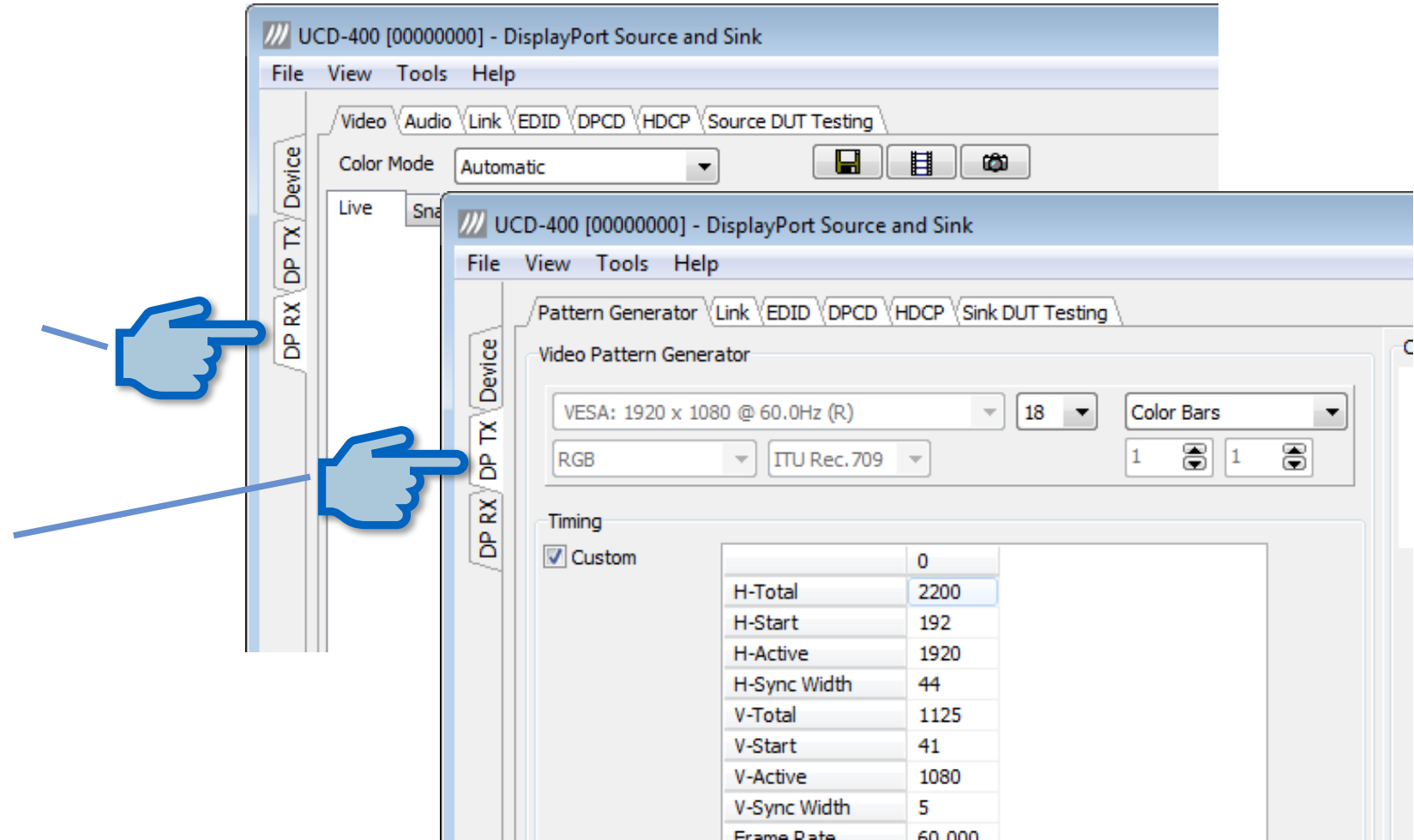
LT with UCD Console

In order to perform Link Training with LTTPRs click here

Thank You!

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