UNIGRAF

DTP-200 Production Test Command specification

Rev. 2.3

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Revision history

Rev.	Date	Author	Description
1.0	17.03.2009	MDe	First version
1.1	20.03.2009	MDe	ACK and NACK syntax changed
1.2	13.05.2009	MDe	Several commands added
1.3	26.05.2009	MDe	Small changes
1.4	20.10.2009	MDe	PT_AUX_LEVEL command added
1.5	25.03.2010	MDe	PT_AUX_LEVEL calibration table added
1.6	24.03.2011	MDe	DPCD and EDID rd/wr commands added
1.7	08.11.2011	MDe	Multibyte DPCD rd/wr commands added
1.8	8.12.2011	MDe	Typos corrected
1.9	23.01.2012	MDe	Several commands added
2.0	13.02.2012	MDe	PT_LINK_STATUS reply updated
2.1	21.03.2013	SG	PT_SET_TIM command updated. Added 1920x1080 and 2560x1440 timings.
2.2	2.06.2016	SG	PT_AUX_LESS_LT and PT_I2CAUX commands added
2.3	27.09.2016	SG	PT_OUT_TP1 and PT_OUT_TP2 commands added

Table of Contents

1. Acronyms and abbreviations

CTS	Compliance Test System
DP	DisplayPort
DPRX	DP Receiver
DPTX	DP Transmitter
DUT	Device Under Test
GUI	Graphical User Interface
I2C	Inter Integrated Circuit bus
LL	Link Layer
PC	Personal Computer
PTCMD	Production Test Command(s)
TBD	To Be Defined
TE	Test Equipment
USB	Universal Serial Bus

2. General

The DPT-200 is a DisplayPort Test Equipment build around the DPTX chip and communicating with a host PC through a RS232 interface. For its operation as production line tester a special set of RS232 commands is used: the Production Test Commands (shortly PTCMDs).

Production Test Commands can be issued by the host using a predefined 115200 Baud rate, 8 bits data, no parity and no handshake format. Every time the DPT-200 receives a command, it replies back to host with an acknowledge message or with an error message.

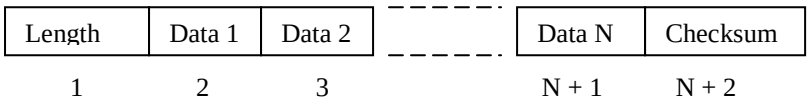
For instance:

HOST		**DPT-200**
Sends “SET_4_LANES”	→	
	←	Replies “ACK”
Sends “SET_LOW_BITRATE”	→	
	←	Replies “ACK”
Sends “SET_6_LANES”	→	
	←	Replies “NACK” (error)

The host must always wait for the DPT-200 reply before issuing the next command.

3. Command syntax

All commands are always formatted in the following way:



- *Length* is the total number of bytes included in the command (N+2).
- *Checksum* is the 2’s complement of the sum of all command bytes from 1 to N+1.

For instance the command:

0x04 0x71 0x1D 0x6E

means:

0x04 = length (command made of 4 bytes)
0x71 = data byte 1
0x1D = data byte 2
0x6E = checksum

Checksum:
0x04 + 0x71 + 0x1D = 0x92
NOT(0x92) + 1 = 0x6D + 1 = 0x6E (2’s complement of 0x92)

Commands sent from the host to the DPT-200 are called ***Requests***. Commands sent from the DPT-200 back to the host are called ***Replies***.

4. PTCMD Requests

4.1. PT_EDID_READ

Offset	Length	Description
0	1	0x07 (length)
1	1	0x72
2	1	0x16 (PT_EDID_READ)
3	1	Segment number (0, 1…)
4	1	Offset (0 – 255, bytes)
5	1	Number of bytes to read (1 – 128)
6	1	Checksum

Reads a number of EDID bytes from the DP sink. A Segment is 256 bytes long. Max 128 bytes can be read for each request.

Replies:

PT_EDID_READ
NACK

4.2. PT_EDID_WRITE

Offset	Length	Description
0	1	Length (7 + N)
1	1	0x72
2	1	0x17 (PT_EDID_WRITE)
3	1	Segment number (0, 1…)
4	1	Offset (0 – 255, bytes)
5	1	Number of bytes to write (1 – 128)
6	N	EDID data
6+N	1	Checksum

Writes a number of EDID bytes to the DP sink. A Segment is 256 bytes long. Max 128 bytes can be written for each request.

Replies:

ACK
NACK

4.3. PT_DPCD_READ

Offset	Length	Description
0	1	0x06 (length)
1	1	0x72
2	1	0x1A (PT_DPCD_READ)
3	2	Address (big endian)
5	1	Checksum

Reads a single byte from the DP sink DPCD memory.

Replies:

PT_DPCD_READ
NACK

4.4. PT_DPCD_WRITE

Offset	Length	Description
0	1	0x07 (length)
1	1	0x72
2	1	0x1B (PT_DPCD_WRITE)
3	2	Address (big endian)
5	1	Data
6	1	Checksum

Writes a single byte to the DP sink DPCD memory.

Replies:
ACK
NACK

4.5. PT_FW_VER

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x1C (PT_SER_NUM)
3	1	0x6E (Checksum)

Gets the TE current firmware version.

Replies:
PT_FW_VER
NACK

4.6. PT_SER_NUM

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x1D (PT_SER_NUM)
3	1	0x6D (Checksum)

Gets the TE serial number.

Replies:
PT_SER_NUM
NACK

4.7. PT_AUX_LEVEL

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x1E (PT_AUX_LEVEL)
3	1	Level (0x00 – 0xFF)
4	1	Checksum

Sets the output voltage level for the AUX channel. The relationship of the parameter value and the achieved output voltage is indicative and according to the following table:

Level	Voltage swing (mVpp)
4	30
8	60
11	80
16	120
24	190
32	260

40	340
48	410
64	570
80	720
96	900
128	1210
160	1510

Replies:
ACK
NACK

4.8. PT_SET_LINK

Offset	Length	Description
0	1	0x0A (length)
1	1	0x72
2	1	0x52 (PT_SET_LINK)
3	1	Skew: 0 = disable 1 = enable
4	1	Scrambling: 0 = disable 1 = enable
5	1	0 = asynchronous clock 1 = synchronous clock
6	1	Enhanced framing: 0 = disable 1 = enable
7	1	Voltage swing level: 0, 1, 2 or 3
8	1	Pre-emphasis level: 0, 1 , 2 or 3
9	1	Checksum

Sets the current DP link parameters.

Replies:
ACK
NACK

4.9. PT_SET_LANES

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x53 (PT_SET_LANES)
3	1	Number of lanes (1, 2 or 4)
4	1	Checksum

Sets the number of lanes used.

Replies:
ACK
NACK

4.10. PT_SET_BRATE

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x54 (PT_SET_BRATE)
3	1	Bitrate (0x06 or 0x0A)
4	1	Checksum

Sets the bitrate used (0x06 = low, 0x0A = high).

Replies:
ACK
NACK

4.11. PT_SET_TIM

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x55 (PT_SET_TIM)
3	1	video timing index (0 to 9)
4	1	Checksum

Sets the index of video timing to use when outputting active video. The supported video timings are listed in Table 1.

Table 1. DPT-200 supported video timings.

Index	Description
0	640 x 480, 27.125 MHz
1	800 x 600, 40 MHz
2	1024 x 768, 65 MHz
3	1280 x 1024, 108 MHz
4	1600 x 1200, 162 MHz
5	1680 x 1050, 119 MHz
6	1920 x 1200, 154 MHz
7	2560 x 1600, 268.5 MHz
8	1280 x 800, 71 MHz
9	1792 x 1344, 204.75 MHz
10	1920 x 1080, 148.5 MHz
11	2560 x 1440, 241.5 MHz

Replies:

ACK
NACK

4.12. PT_SET_PATT

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x56 (PT_SET_PATT)
3	1	video pattern index (0 to 26)
4	1	Checksum

Sets the index of video pattern to use when outputting active video. The supported video patterns are listed in Table 2.

Table 2. DPT-200 supported video patterns.

Index	Description
0	Checkboard 1
1	Checkboard 2
2	Checkboard 3 (black and white)
3	RGBW 16-lines stripes
4	RGBW big stripes
5	Coarse grid
6	Red vertical stripes (2 pixels red, 2 pixel black)
7	Green vertical stripes (2 pixels green, 2 pixel black)
8	Blue vertical stripes (2 pixels blue, 2 pixel black)
9	White vertical stripes (2 pixels white, 2 pixel black)
10	Red horizontal stripes (2 pixels red, 2 pixel black)
11	Green horizontal stripes (2 pixels green, 2 pixel black)
12	Blue horizontal stripes (2 pixels blue, 2 pixel black)
13	White horizontal stripes (2 pixels white, 2 pixel black)
14	Blue H-Slide
15	Green H-Slide
16	Red H-Slide
17	White H-Slide
18	Blue coarse H-Slide
19	Green coarse H-Slide
20	Red coarse H-Slide

21	White coarse H-Slide
22	Solid white
23	Solid red
24	Solid green
25	Solid blue
26	Solid black

Replies:
ACK
NACK

4.13. PT_OUT_IDLE

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x57 (PT_OUT_IDLE)
3	1	0x33 (Checksum)

Outputs idle pattern.

Replies:
ACK
NACK

4.14. PT_OUT_VIDEO

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x58 (PT_OUT_VIDEO)
3	1	0x32 (Checksum)

Outputs active video.

Replies:
ACK
NACK

4.15. PT_OUT_TP1

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x67 (PT_OUT_TP1)
3	1	0x23 (Checksum)

Outputs TP1 training pattern (same as D10.2)

Replies:
ACK
NACK

4.16. PT_OUT_TP2

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x68 (PT_OUT_TP2)
3	1	0x22 (Checksum)

Outputs TP2 training pattern

Replies:

ACK
NACK

4.17. PT_OUT_D102

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x59 (PT_OUT_D102)
3	1	0x31 (Checksum)

Outputs D10.2 pattern.

Replies:

ACK
NACK

4.18. PT_OUT_PRBS7

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x5A (PT_OUT_PRBS7)
3	1	0x30 (Checksum)

Outputs PRBS7 pattern.

Replies:

ACK
NACK

4.19. PT _DPCD_NREAD

Offset	Length	Description
0	1	0x08 (length)
1	1	0x72
2	1	0x5B (PT _DPCD_NREAD)
3	3	Address (little endian)
6	1	Length (1-16)
7	1	Checksum

Reads 1 to 16 bytes from the DP sink DPCD memory.

Replies:

PT _DPCD_NREAD
NACK

4.20. PT _DPCD_NWRITE

Offset	Length	Description
0	1	Length (8+N)
1	1	0x72
2	1	0x5C (PT _DPCD_NWRITE)
3	3	Address (little endian)
6	1	Length N (1-16)
7	N	Data
7+N	1	Checksum

Writes 1 to 16 bytes to the DP sink DPCD memory.

Replies:

ACK
NACK

4.21. PT_START_LT

Offset	Length	Description
0	1	0x0C (length)
1	1	0x72
2	1	0x5D (PT_START_LT)
3	1	0x06 = low bitrate 0x0A = high bitrate
4	1	1, 2 or 4 lane count
5	1	0 = skew disable 1 = skew enable
6	1	0 = no scrambling 1 = scrambling
7	1	0 = asynchronous clock 1 = synchronous clock
8	1	0 = normal framing 1 = enhanced framing 3 = auto
9	1	Scrambler Reset: 0 = 0xFFFF (DP) 1 = 0xFFFE (eDP) 3 = auto
10	1	eDP Framing Change: 0 = disabled 3 = auto
11	1	Checksum

Starts link training. The reply reflects command acceptance, not a successful link training event.

Replies:
ACK
NACK

4.22. PT_PWR_ON

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x5E (PT_PWR_ON)
3	1	0x2C (Checksum)

Powers on the main link and writes 1 to DPCD 00600h to issue a Power Save Exit request.

Replies:
ACK
NACK

4.23. PT_PWR_OFF

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x5F (PT_PWR_OFF)
3	1	0x2B (Checksum)

Powers off the main link and writes 2 to DPCD 00600h to issue a Power Save Entry request.

Replies:
ACK
NACK

4.24. PT_FAST_LT

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x60 (PT_FAST_LT)
3	1	0x2A (Checksum)

Performs a Fast Link Training using link parameters currently set (lane count, link rate, swing and pre-emphasis) in the DPCD.

Replies:
ACK
NACK

4.25. PT_LINK_STATUS

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0xA1 (PT_LINK_STATUS)
3	1	0xE9 (Checksum)

Gets the current DP link status.

Replies:
PT_LINK_STATUS
NACK

4.26. PT_HDCP_STATUS

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0xA3 (PT_HDCP_STATUS)
3	1	0xE7 (Checksum)

Gets the current Main Stream Attributes.

Replies:
PT_HDCP_STATUS
NACK

4.27. PT_USER_TIM

Offset	Length	Description
0	1	0x1C (length)
1	1	0x72
2	1	0x61 (PT_USER_TIM)
3	2	H_TOTAL (pixels)
5	2	H_SYNC_WIDTH (pixels)
7	2	H_BACKPORCH (pixels)
9	2	H_ACTIVE (pixels)
11	2	V_TOTAL (lines)
13	2	V_SYNC_WIDTH (lines)
15	2	V_BACKPORCH (lines)
17	2	V_ACTIVE (lines)
19	4	PIXEL_CLOCK (kHz)
23	1	TEST_MISC_1
24	1	0x00
25	1	0x00
26	1	0x00
27	1	Checksum

Forces the DP source to use the specified timing and the internal timing/pattern generator. Invoked with PIXEL_CLOCK = 0 switches back to the external input video signal.

TEST_MISC_1:
Bit[0]: set to 0
Bit[2:1]: “00” = RGB, “01” = YCbCr 4:2:2, “10” = YCbCr 4:4:4
Bit[3]: 0 = VESA range, 1 = CEA range
Bit[4]: 0 = ITU601 colors, 1 = ITU709 colors

Bit[7:5]: “000” = 6bpc, “001” = 8bpc, “010” = 10bpc

Replies:
ACK
NACK

4.28. PT_AUDIO_TX_STATUS

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x62 (PT_AUDIO_TX_STATUS)
3	1	0x28 (Checksum)

Queries the current audio status.

Replies:
PT_AUDIO_TX_STATUS
NACK

4.29. PT_HDCP_ENABLE

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x63 (PT_HDCP_ENABLE)
3	1	0 = disable 1 = enable
4	1	Checksum

Enables or disables HDCP (Content Protection, CP).

Replies:
ACK
NACK

4.30. PT_AUX_LESS_LT

Offset	Length	Description
0	1	0x0A (length)
1	1	0x72
2	1	0xAC (PT_AUX_LESS_LT)
3	1	LINK_BW_SET
4	1	LANE_COUNT_SET
5	1	SCRAMBLING
6	1	VOLTAGE_SWING
7	1	PRE_EMPHASIS
8	1	Timeout (s)
9	1	Checksum

Executes AUX-less link training procedure.

LINK_BW_SET
0x06 1.62 Gbps per lane
0x0A 2.7 Gbps per lane

LANE_COUNT_SET
Bit 4:0
00000b 1 lane
00010b 2 lanes
00100b 4 lanes

Bit 6:5
Reserved, set to 0.
Bit 7
0 Enhanced framing not supported
1 Enhanced framing supported

SCRAMBLING
0x00 Scrambling disabled
0x01 Scrambling enabled

VOLTAGE_SWING
0x00 Voltage swing level 0
0x01 Voltage swing level 1
0x02 Voltage swing level 2
0x03 Voltage swing level 3

PRE_EMPHASIS
0x00 Pre-emphasis level 0
0x01 Pre-emphasis level 1
0x02 Pre-emphasis level 2
0x03 Pre-emphasis level 3

Timeout
Maximum length of time (in seconds) that command execution can take. ACK reply is sent when link is established or timeout expires. Use PT_LINK_STATUS command to read link status information.

Replies:
ACK
NACK

4.31. PT_I2CAUX_WR_RD

Offset	Length	Description
0	1	Length (7+N)
1	1	0x72
2	1	0x64 (PT_I2CAUX_WR_RD)
3	1	I2C device address
4	1	Number of bytes to write (0-128)
5	1	Number of bytes to read (0-128)
6	N	Write data
6+N	1	Checksum

Executes I2C Write followed by Repeated Start followed by I2C Read followed by Stop. If Number of bytes to read is set to 0 then only I2C Write followed by Stop is executed. If number of bytes to write is set to 0 then only I2C Read followed by Stop is executed.

Replies:
PT_I2C_AUX_WR_RD
NACK

Examples:
08 72 64 A0 01 80 00 01 - read first EDID block
08 72 64 A0 01 80 80 81 - read second EDID block

4.32. PT_I2CAUX_RD_REQ

Offset	Length	Description
0	1	0x07 (length)

1	1	0x72
2	1	0x65 (PT_I2CAUX_RD_REQ)
3	1	Device address
4	1	Stop: 0 – middle of transaction 1 – complete transaction with Stop condition
5	1	Length (1-16)
6	1	Checksum

Sends I2C over AUX read request.

Replies:
PT_I2CAUX_RD_REQ
NACK

Examples:
07 72 65 A0 00 10 72 - read 16 bytes EDID
07 72 65 A0 01 00 81 - stop condition

4.33. PT_I2CAUX_WR_REQ

Offset	Length	Description
0	1	Length (7+N)
1	1	0x72
2	1	0x66 (PT_I2CAUX_WR_REQ)
3	1	Device address
4	1	Stop: 0 – middle of transaction 1 – complete transaction with Stop condition
5	1	Length N (1-16)
6	N	Data
6+N	1	Checksum

Sends I2C over AUX write request.

Replies:
PT_I2CAUX_WR_REQ
NACK
Example:
08 72 66 A0 00 01 80 FF - select second EDID block

5. Replies

5.1. ACK

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x0C (ACK)
3	1	0x7E (Checksum)

5.2. NACK

Offset	Length	Description
0	1	0x04 (length)
1	1	0x72
2	1	0x0B (NACK)
3	1	0x7F (Checksum)

5.3. PT_EDID_READ

Offset	Length	Description
0	1	Length (4 + N)
1	1	0x72
2	1	0x16 (PT_EDID_READ)

3	N	EDID data
3+N	1	Checksum

5.4. PT_DPCD_READ

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x1A (PT_DPCD_READ)
3	1	Data read
4	1	Checksum

5.5. PT_FW_VER

Offset	Length	Description
0	1	0x07 (length)
1	1	0x72
2	1	0x1C (PT_FW_VER)
3	1	Major
4	1	Minor
5	1	Revision
6	1	Checksum

5.6. PT_SER_NUM

Offset	Length	Description
0	1	0x0C (length)
1	1	0x72
2	1	0x1D (PT_SER_NUM)
3	8	Serial number
11	1	Checksum

5.7. PT _DPCD_NREAD

Offset	Length	Description
0	1	Length (4+N)
1	1	0x72
2	1	0x5B (PT _DPCD_NREAD)
3	N	Data read
3+N	1	Checksum

5.8. PT_LINK_STATUS

Offset	Length	Description
0	1	0x15 (length)
1	1	0x72
2	1	0xA1 (PT_LINK_STATUS)
3	1	LANE0_1_STATUS
4	1	LANE2_3_STATUS
5	1	L0 voltage swing (0, 1, 2, 3)
6	1	L1 voltage swing (0, 1, 2, 3)
7	1	L2 voltage swing (0, 1, 2, 3)
8	1	L3 voltage swing (0, 1, 2, 3)
9	1	L0 pre-emphasis (0, 1, 2, 3)
10	1	L1 pre-emphasis (0, 1, 2, 3)
11	1	L2 pre-emphasis (0, 1, 2, 3)
12	1	L3 pre-emphasis (0, 1, 2, 3)
13	1	Lane count (0, 1, 2 or 4)
14	1	0x06 = low bitrate 0x0A = high bitrate
15	1	0 = normal framing 1 = enhanced framing
16	1	0 = skew disabled 1 = skew enabled
17	1	0 = scrambling disabled 1 = scrambling enabled
18	1	Scrambler Reset: 0 = 0xFFFF (DP) 1 = 0xFFFE (eDP)
19	1	eDP Framing Change: 0 = disabled 1 = enabled
20	1	Checksum

LANE0_1_STATUS:

coding as DPCD location 0x202

LANE2_3_STATUS:
coding as DPCD location 0x203

Voltage swing:
0 = 400 mVpp
1 = 600 mVpp
2 = 800 mVpp
3 = 1.2 Vpp
Pre-emphasis:
0 = 0 dB
1 = 3.5 dB
2 = 6 dB
3 = 9.5 dB

5.9. PT_AUDIO_TX_STATUS

Offset	Length	Description
0	1	0x11 (length)
1	1	0x72
2	1	0x62 (PT_AUDIO_TX_STATUS)
3	1	IN_STATE
4	1	IN_CH_COUNT
5	1	IN_SAMPLE_SIZE
6	1	IN_SAMPLE_FREQ LSB
7	1	IN_SAMPLE_FREQ
8	1	IN_SAMPLE_FREQ
9	1	IN_SAMPLE_FREQ MSB
10	1	ACS BYTE 0
11	1	ACS BYTE 1
12	1	ACS BYTE 2
13	1	ACS BYTE 3
14	1	ACS BYTE 4
15	1	ACS BYTE 5
16	1	Checksum

IN_STATE: Input state
bit 1:0: 00 = no input signal, 01 = unlocked, 10 = locked.

IN_CH_COUNT: Input channel count (0 – 8).

IN_SAMPLE_SIZE: Input sample size (bits, 16 – 24).

IN_SAMPLE_FREQ: Input sample frequency (in Hz, 32-bit wide, little endian).

ACS: Input Audio Channel Status (IEC-60958 / IEC-61937)
ACS[0]:
bit 1:0: standard 00 = “IEC-60958-3” 01 = “IEC-60958-4”
10 = “IEC-61937” 11 = “SMPTE-337M”
ACS[0]:
bit 0: use. 0 = consumer, 1 = professional
bit 1: coding. 0 = LPCM, 1 = compressed
bit 2: copyright. 0 = yes, 1 = no
bit 7:6: mode (0 – 3)
ACS[1]:
bit7:0: Category code (0 – 0xFF).
ACS[2]:
bit3:0: Source number (0 – 15)
bit7:4: Channel number (0 – 15)
ACS[3]:
Bit5:4: Clock accuracy (0 = Level II, 1 = Level I, 2 = Level III,
3 = Interface frame rate not matched to sample frequency)

If IN_STATE(1:0) is different from “locked”, the rest of the status data is invalid.

If ACS[0] bits 1:0 are different from 00 and 10, only the standard used and ACS[0-5] raw hex data should be displayed (channel count, sample size and sampling frequency are invalid too

5.10. PT_HDCP_STATUS

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0xA3 (PT_HDCP_STATUS)
3	1	0 = not authenticated 1 = authenticated
4	1	HDCP_TX_STAT
5	1	Checksum

Current status of HDCP authentication.

HDCP_TX_STAT (defined only for DP source TEs):
- bit 0: CP_required
- bit 1: receiver_sensed
- bit 2: HDCP_capability
- bit 3: repeater
- bit 4: error_generic

5.11. PT_I2CAUX_WR_RD

Offset	Length	Description
0	1	Length (5+N)
1	1	0x72
2	1	0x64 (PT_I2CAUX_WR_RD)
3	1	Number of bytes read (0-128)
4	N	Read data
4+N	1	Checksum

5.12. PT_I2CAUX_RD_REQ

Offset	Length	Description
0	1	Length (5+N)
1	1	0x72
2	1	0x65 (PT_I2CAUX_RD_REQ)
3	1	Number of bytes read (0-16)
4	N	Read data
4+N	1	Checksum

5.13. PT_I2CAUX_WR_REQ

Offset	Length	Description
0	1	0x05 (length)
1	1	0x72
2	1	0x66 (PT_I2CAUX_WR_REQ)
3	1	Number of bytes written
4	1	Checksum